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(54) Title: PHASE-LOCKED LOOP WITH INCREMENTAL PHASE DETECTORS AND A CONVERTER FOR COMBINING A LOGICAL OPERATION WITH A DIGITAL TO ANALOG CONVERSION
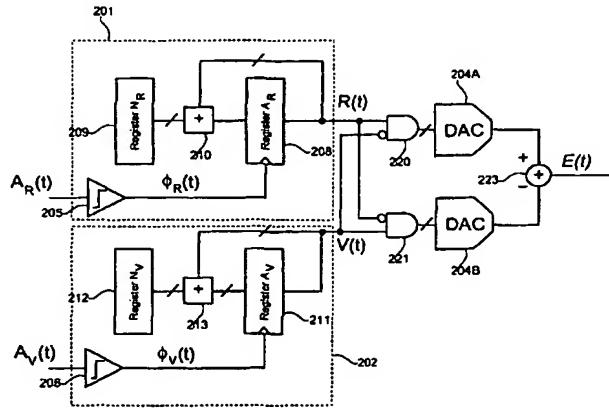
(57) Abstract: The invention relates to a phase-locked loop comprising a voltage controlled oscillator and having a frequency control input for controlling the frequency of the output signal. The phase-locked loop also has a phase comparator for deriving a control signal from a phase error detected in response to a received output signal and a reference signal. The control signal is coupled to the frequency control input of said voltage controlled oscillator. The phase comparator includes a first and a second predefined phase step value to a first accumulated phase value, and the phase comparator has means for determining the phase error. The phase comparator may further have circuit means for performing a first and a second AND operation on the outputs from the first and second accumulators and for obtaining analogue signals corresponding to the outputs of the AND operations. The invention also relates to a method for obtaining information on a phase error between two signals. The invention also relates to a phase comparator for use in a phase-locked loop. The invention further relates to a digital to analogue converter, which converter may combine a logic operation with a digital to analogue conversion.

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PHASE-LOCKED LOOP WITH INCREMENTAL PHASE DETECTORS AND A
CONVERTER FOR COMBINING A LOGICAL OPERATION WITH A DIGITAL TO
ANALOGUE CONVERSION

5   FIELD OF THE INVENTION

The present invention relates to a phase-locked loop, and more particularly to a
phase-locked loop having a phase comparator with a phase error being derived from
the outputs of incremental phase detectors.

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The invention also relates to a method for determining a phase error in response to
a first signal and a second signal and a phase comparator for carrying out the
method.

15   The present invention further relates to a digital to analogue converter, and more
particularly to a converter for combining a logical operation with a digital to analogue
conversion.

BACKGROUND OF THE INVENTION

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Phase-locked loops are used in a variety of applications. In general, phase-locked
loops include a phase comparator or phase detector to compare the phase of a
frequency-divided output signal of the voltage controlled oscillator and a reference
signal. The difference between these two signals is used to generate a control signal

25   or error signal, which is fed back to the voltage controlled oscillator so as to control
the frequency of its signal output in a direction that reduces this phase difference.
For example, phase-locked loops are used in different types of radio systems, such
as cellular phones, in which an oscillator is locked to an accurate reference
frequency. Different means are then provided to scale this accurate reference

30   frequency to the desired frequency.

In a conventional phase-locked loop (PLL) it is well known to divide the output signal
of the voltage controlled oscillator (VCO) by a natural number. The division may be
performed by a divider or frequency divider. The reason to perform the division is

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because comparators according to the prior art only are able to compare the phase of two signals if the frequency of the two signals to be compared are equal and because the output frequency usually is "high" (MHz or GHz range) it is easier/more feasible to have the control circuit to work at a lower frequency. In some

5   embodiments the reference clock may also be divided by a natural number by a frequency divider in order to obtain a given frequency of the two signals to be compared.

When using a conventional phase-locked loop some unwanted frequency

10   components or spurious occur in the output signal. These spurious occur as a result of the phase comparator (also called phase detector) working at a frequency given hereby. The spurious are an unwanted effect as it most often reduces the overall performance of the system in which the phase-lock loop is operating. For example, spurious on the carrier in a radio system is a disadvantage as it causes undesired

15   channels to interfere with the desired channel and thereby reducing the over-all performance of the radio system.

According to the prior art, a solution to this problem is to filter out the spurious by use of a loop filter, most often located between the phase comparator and the

20   voltage-controlled oscillator, i.e. the control signal for the voltage-controlled oscillator is filtered. Generally the spurious can be filtered out in a loop filter if the bandwidth of the loop filter is significantly small, e.g. smaller than the distance between the spurious. But the price of reducing the bandwidth of the loop filter is a slower PLL, i.e. the lock-in time for the PLL is increased.

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Some if not most prior art phase-locked loops, which are fully or partly implemented using digital components, also have a risk of producing sub-harmonic frequencies due to the way they are implemented. This is due to the way the two signals, the reference signal and the output signal, interact with each other. Ideally the reference

30   signal and the output signal operates asynchronous, where the phase lock is established when the phases coincide. Until this happens and if a disturbance breaks the lock there may occur sub-harmonics.

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US 5459435 shows a digital implementation of a PLL. The invention is a straight forward conversion of the known analog PLL topology, where a first and a second counter unit is used to indicate the phase error between the frequency divided output signal and the reference. The resolution of the PLL is fixed to the bit

5   resolution of the digital implementation thus fixing the ratios between output frequency and reference frequency.

US 5999060 also shows a digital implementation of a PLL using counters. As with US 5459435 the resolution of the PLL is firstly fixed to the bit resolution, but is

10   secondly compensated by a scaling means in the feed back. The scaling means gives the possibility to increase the number of possible output frequencies.

US 6188288 is similar in many ways to US 5999060 in that some scaling means is used in the feed back to compensate for the bit resolution. US 6188288 differs from

15   the above mentioned PLL's in that a current controlled oscillator is used and not a voltage controlled oscillator.

The above mentioned PLL introduces means for increasing the number of possible output frequencies. They also increase the complexity of the PLL-circuit

20   considerably and do not improve on the lock-in time for the PLL, because a loop filter with a narrow bandwidth is still needed.

In US 6046643 is described a digital implementation of a PLL circuit. Here, a frequency divider with a fixed division rate has the output of the voltage controlled

25   oscillator as input, and the output of the divider supplies a first clock signal to a first accumulator, which aggregates a first reference signal under control of the first clock signal. A second accumulator aggregates a second reference signal under the control of the reference clock signal. The aggregated signals are subtracted from one another, filtered through a digital filter, weighted and then converted into an

30   analogue signal. This analogue signal is filtered by an analogue filter and fed to the voltage controlled oscillator. Thus, the difference between the two aggregated signals may be used for generating a control or error signal for controlling the frequency of the voltage controlled oscillator in a direction to reduce the difference between the two aggregated signals, and the output frequency may be selected by a

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suitable selection of the first and second reference signals. However, the two aggregated signals from the two accumulators are asynchronous signals, thereby generating a problem for the subtraction process. In US 6046643 there is nowhere giving a solution for performing such a subtraction of two asynchronous signals,

5   except for the filtering processes following the subtraction.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an improved phase-locked loop,

10   which may have a fast lock-in time, minimum risk for sub-harmonics in the output, and which can be implemented in a simple circuit.

It is also an object of the present invention to provide a solution to the subtraction of two asynchronous digital signals to obtain a phase error signal, which may be used

15   to obtain an improved phase-locked loop circuit.

In order to provide the phase error signal, an analogue signal may be obtained from the two subtracted asynchronous digital signals, which may include the use of one or more digital to analogue converters. Thus, it is also an object of the invention to

20   provide a solution to a converter circuit for obtaining an analogue presentation of one or more digital input signals.

According to a first aspect of the invention, there is provided a phase-locked loop comprising:

25   a voltage controlled oscillator for generating an output signal and having a frequency control input for controlling the frequency of the output signal, and
a phase comparator for deriving a control signal from a phase error detected in response to the received output signal and a reference signal, said control signal being coupled to the frequency control input of said voltage controlled oscillator,

30   wherein the phase comparator includes:
a first accumulator adapted to add a first predefined phase step value to a first accumulated phase value in response to a reoccurring event in the reference signal,

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a second accumulator adapted to add a second predefined phase step value to a second accumulated phase value in response to a reoccurring event in the received output signal, and

means or arithmetic means for determining the phase error from the obtained first
5   and second accumulated phase values.

According to an embodiment of the invention, the means for determining the phase error from the obtained first and second accumulated phase values may be adapted to derive the control signal based on the obtained phase error or to derive the
10   control signal from the obtained first and second accumulated phase values, whereby the control signal may represent the phase error.

A PLL of this type may have a large loop-bandwidth, which is independent of the division ratio and consequently a fast lock-in time. The loop-bandwidth may be large
15   because, as shown later, the spurious in the output to a large degree may be placed as desired, thus allowing for a loop-filter with a wider bandwidth.

Because the loop-bandwidth may be larger, the time-constant of the loop may be smaller. Therefore it may be cheaper to integrate a PLL of this type because the
20   sizes of the loop-components are smaller and thereby take up a smaller die array.

Because the loop-bandwidth may be independent of the division ratio, the PLL can compensate for frequency errors in references, and thereby eliminate the need of using voltage controlled temperature compensated crystal oscillators (VCTXCO) or
25   voltage controlled crystal oscillators (VCXO), which is used in nearly all wireless radio systems and other communications systems. VCTCXO and VCXO is normally an expensive circuit and can be replaced with a more simple crystal oscillator which normally has better phase noise performance than VCTCXO and VCXO.

30   Also, because the loop-bandwidth may be larger it is possible to suppress narrowband phase noise of the VCO in a wider bandwidth around the carrier and hereby improving the overall performance of the PLL. This means that VCO does not have to have as good narrowband phase-noise performance as for a traditional PLL system. Because resonators on an integrated circuit has very low Q-values, the

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performance of integrated VCO are usually not as good as a discreet solution. In some systems this gives the possibility to fully integrate the VCO where it would not be possible using a traditional system.

5   Further, because the PLL may have a fast lock-in time, it is possible to direct-digital-modulate the PLL by changing the predefined phase step values (N_R and N_V). This means that the up-converter can be eliminated in systems using frequency shift keying (FSK) and phase shift keying (PSK).

10   According to a preferred embodiment of the invention the phase-locked loop may further comprise a divider for dividing the frequency of the output signal, whereby the received output signal received by the phase comparator is a frequency-divided output signal.

15   It is preferred that the arithmetic means are subtracting means for determining the phase error by a subtraction between the obtained first and second accumulated phase values. Here, the subtracting means may be adapted for subtracting the second accumulated phase value from the first accumulated phase value.

20   According to a preferred embodiment of the invention, the phase comparator includes a digital-to-analogue converter adapted to convert the phase error and thereby to generate an analogue output signal. Hereby the phase-locked loop may achieve a very large internal amplification – an amplification that approaches infinite – so the bandwidth of the phase-locked loop is determined primarily by the loop filter.

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It is also within a preferred embodiment of the invention that the phase comparator includes a converter circuit having:
means for performing a first logic bit by bit AND operation of the output of the first accumulator and the inverted output of the second accumulator, and for generating
30   a first analogue representation of said first logic bit by bit AND operation, and means for performing a second logic bit by bit AND operation of the output of the second accumulator and the inverted output of the first accumulator, and for generating a second analogue representation of said second logic bit by bit AND operation.

Here, the converter circuit may comprise current mode logic circuits giving a current output for a two input AND operation, and the current output may be used for generating an analogue representation for a bit by bit AND operation. It is preferred

5   that the arithmetic means are adapted to obtain one or two analogue phase error signals based on the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation. The arithmetic means may comprise subtraction means being adapted for performing an analogue subtraction of the second analogue representation from the

10   first analogue representation.

According to a preferred embodiment of the invention, the phase comparator includes a first and a second digital-to-analogue converter adapted to convert the first and the second accumulated phase values and thereby to generate analogue

15   representations thereof. It is further preferred that arithmetic means are adapted to perform an analogue subtraction of the analogue representation of the second accumulated phase value from the analogue representation of the first accumulated phase value. This may be advantageous due the fact that the reference signal and the output signal essentially operate asynchronously. Due to the way a digital

20   subtraction may be carried out, it may be difficult to implement an asynchronously digital subtraction which will operate momentously or need to operate momentously without generating spikes or hazards on the output, which may cause spurious or in worst case mall function.

25   According to a preferred embodiment of the invention, the phase comparator includes a first and a second AND-means, where the output of said first AND-means is connected to a first digital-to-analogue converter, whereby a first accumulator is connected to a first non-inverting input of said first AND-means and whereby a second accumulator is connected to a first inverting input of said first AND-means,

30   the output of said second AND-means being connected to said second digital-to-analogue converter, and that said second accumulator further is connected to a first non-inverting input of said second AND-means, said first accumulator further being connected to a first inverting input of said second AND-means. The digital-to-analogue converters have a settling time - the time from a digital input is applied to

the digital-to-analogue converter until a stable output is achieved - which may cause large but short lived errors when the more-significant bit changes, especially the most significant bit. This is especially a problem, because the reference signal and the output signal essentially operate asynchronously. Furthermore, due to the way

5   digital addition (subtraction) is done inside the component, there may be a short ripple in the output from the component. By using an AND-means, the digital number is pre-processed, facilitating a more error-free output from the digital-to-analogue converter.

10   According to a preferred embodiment of the invention, the phase comparator includes a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator, and a third AND-means, where the output of said third AND-means is connected to said first and said second reset means of said first and said second accumulator, where

15   the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means. The intended output from the phase comparator is the phase difference between the two signals and not their absolute value. By using reset means for the most

20   significant bit of said first and second accumulator numerical overflows of the accumulators may be prevented and at the same time the output from the phase comparator may remain the same. As described above, the most significant bits of the accumulator are reset and the resetting is controlled by the most significant bits of the inputs to the digital-to-analogue converter. The same function may be

25   achieved by using any of the bits and any number of resets.

The invention also relates to a method of detecting a phase error between or in response to a first signal and a second signal. Thus, according to a second aspect of the invention there is provided a method for determining a phase error in

30   response to a first signal and a second signal, said method comprising the steps of: generating a first reoccurring trigger event in response to the first signal, generating a second reoccurring trigger event in response to the second signal, incrementing a first phase value by a first predetermined increment value when the first trigger event occurs to obtain a first accumulated phase value,

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incrementing a second phase value by a second predetermined increment value when the second trigger event occurs to obtain a second accumulated phase value, and

calculating or determining said phase error based on obtained first and second
5   accumulated phase values.

The method of the invention may also comprise the step of frequency dividing the first signal and/or the second signal, whereby the generation of the first and/or second reoccurring trigger event is performed in response to the frequency divided
10   first and/or second signal, respectively.

It is preferred that the calculation or determination of the phase error is based on a subtraction of said second accumulated phase value from said first accumulated phase value.

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According to an embodiment of the method of the invention, the first accumulated phase value, the second accumulated phase value and the phase error are represented by binary numbers.

20   However, it is preferred that the first accumulated phase value and the second accumulated phase value are represented by binary numbers and the phase error is represented by one or more an analogue signals. Here, the method of the invention may further comprise the steps of:

performing a first logic bit by bit AND operation of the first accumulated phase value
25   and the inverted second accumulated phase value, and generating a first analogue representation of said first logic bit by bit AND operation, and

performing a second logic bit by bit AND operation of the second accumulated phase value and the inverted first accumulated phase value, and generating a second analogue representation of said second logic bit by bit AND operation.

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According to an embodiment of the invention, the calculation or determination of the phase error may comprise generating one or two analogue phase error signals based on the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND

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operation. Here, the calculation or determination of the phase error may comprise performing an analogue subtraction of the second analogue representation from the first analogue representation.

5   It is within an embodiment of the method of the invention that the most significant bit of the first accumulated phase value and the most significant bit of the second accumulated phase value are reset when the most significant bit of both said first accumulated phase value and said second accumulated phase value are simultaneously 1 or logic high. It is also within an embodiment that two equal bits of

10   the first and second accumulated phase values are reset whenever these bits are 1 or logic high at the same time.

According to the second aspect of the invention there is also provided a phase comparator for carrying out the method or methods of the second aspect of the

15   invention. Here the first signal is a reference signal and the second signal is an input signal, and the phase comparator comprises:
a first accumulator adapted to add a first predefined phase step value to a first accumulated phase value in response to a reoccurring event in said reference signal,

20   a second accumulator adapted to add a second predefined phase step value to a second accumulated phase value in response to a reoccurring event in said input signal, and
means or arithmetic means for determining the phase error based on the second accumulated phase value and the first accumulated phase value.

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Here, the arithmetic means may comprise subtracting means for determining the phase error by subtracting the second accumulated phase value from the first accumulated phase value.

30   According to an embodiment of the invention, the phase comparator may include a digital-to-analogue converter adapted to convert the phase error and thereby to generate an analogue output signal.

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It is within a preferred embodiment that the phase comparator includes a converter circuit having:

means for performing a first logic bit by bit AND operation of the output of the first accumulator and the inverted output of the second accumulator, and for generating

5   a first analogue representation of said first logic bit by bit AND operation, and means for performing a second logic bit by bit AND operation of the output of the second accumulator and the inverted output of the first accumulator, and for generating a second analogue representation of said second logic bit by bit AND operation. Here, the converter circuit may comprise current mode logic circuits

10   giving a current output for a two bit AND operation, said current output being used for generating an analogue representation for a bit by bit AND operation.

According to an embodiment of the phase comparator of the invention, the arithmetic means may be adapted to obtain one or two analogue phase error signals

15   based on the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation. Here, the arithmetic means may comprise subtraction means being adapted for performing an analogue subtraction of the second analogue representation from the first analogue representation.

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It is also within an embodiment of the phase comparator of the invention that the phase comparator includes a first and a second digital-to-analogue converter adapted to convert the first and the second accumulated phase values and thereby to generate analogue representations thereof. Here, it is preferred that the arithmetic

25   means are adapted to perform an analogue subtraction of the analogue representation of said second accumulated phase value from the analogue representation of said first accumulated phase value.

The second aspect of the invention also includes a phase comparator, wherein the

30   phase comparator includes a first and a second AND-means, where the output of said first AND-means is connected to a first digital-to-analogue converter, whereby a first accumulator is connected to a first non-inverting input of said first AND-means, and whereby a second accumulator is connected to a first inverting input of said first AND-means, the output of said second AND-means being connected to said second

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digital-to-analogue converter, and that said second accumulator further is connected to a first non-inverting input of said second AND-means, said first accumulator further being connected to a first inverting input of said second AND-means.

5   The second aspect of the invention also comprises an embodiment of a phase comparator, wherein the phase comparator includes a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator and a third AND-means, where the output of said third AND-means is connected to said first and said second reset means of said first and

10   said second accumulator, where the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means.

15   According to a third aspect of the invention there is provided a converter circuit for obtaining an analogue presentation of a digital input signal or of a logical operation on several digital input signals, at least one of the digital input signals having at least 2 bits, said circuit comprising:
       a number of current mode logic circuits, CML circuits arranged in modules, with

20   each CML circuit having one or more logic input signals, a first current line, a second current line and a constant current source, each of said CML circuits further comprising means for switching the constant current source between a first conductive state, in which the current source draws or delivers current via the first current line, and a second conductive state, in which the current source draws or

25   delivers current via the second current line, said switching being controlled by at least one of the logic input signals, wherein
       a first module has at least one CML circuit, with each CML circuit of the first module having a first logic input signal representing the first bit value of a first digital input signal and providing a first control signal for the switching between the first and the

30   second conductive state, and
       a second module has at least one CML circuit, with each CML circuit of the second module having a first logic input signal representing the second bit value of the first digital input signal and providing a first control signal for the switching between the first and the second conductive state.

According to an embodiment of the converter circuit of the invention, the first digital signal may have N-bits, wherein for each bit k, where k is selected as an integer larger than or equal to zero and smaller than or equal to N-1, there is a

5   corresponding module k having at least one CML circuit, with each CML circuit of the module k having a first logic input signal representing the value of the corresponding bit k of the first digital input signal and providing a first control signal for the switching between the first and the second conductive state.

10   It is preferred that the current drawn from or delivered to said first current lines of the CML circuits arranged in the modules is used for generating a first analogue output for the converter circuit.

According to an embodiment of the converter circuit, at least part or all of the CML

15   circuits have said logic input signals together with the inverse of said logic input signals as input signals for controlling the switching between the first and the second conductive state.

According to an embodiment of the converter circuit, then for each module k, there

20   is one corresponding CML circuit. Here, the current drawn from or supplied to the first lines of the CML circuits of the modules may be used for generating the first analogue output as a voltage output via a first resistor network or via a first capacitor network.

25   According to another embodiment of the converter circuit, then for each module k, there are 2^k corresponding CML circuits. Here, the sum of the current drawn from or supplied to the first lines of the CML circuits of the modules may be used for generating the first analogue output as a current output.

30   For the converter circuit of the invention, it is preferred that for the first module, the logic of each CML circuit is designed so that in order for the first logic input signal to control the state of a CML circuit to be in the first conductive state, the first bit of the first digital signal shall be active or logic high. It is also preferred that for the second module, the logic of each CML circuit is designed so that in order for the first logic

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input signal to control the state of a CML circuit to be in the first conductive state, the second bit of the first digital signal shall be active or logic high.

5   In general it is preferred that for a converter circuit having a module k, the logic of each CML circuit is designed so that in order for the first logic input signal to control the state of a CML circuit to be in the first conductive state, the corresponding bit k of the first digital signal shall be active or logic high.

10   According to an embodiment of the third aspect of the invention, a part or all of the CML circuits of said modules may be designed as buffer or inverter circuits having only one logic input signal together with the inverse of said logic signal, said logic signal representing a corresponding bit of the first digital signal.

15   The CML circuits of the converter circuit of the third aspect of the present invention may be designed to perform different logic functions such as AND, NAND, OR, NOR, XOR or XNOR functions, and the CML circuits may have a number of corresponding logic input signals together with the inverse of such logic signals. When using a complementary CML circuitry, the circuitry used for performing AND, NAND, OR or NOR functions is very much the same, the resulting function being 20   determined by how the input signals and their inverse signals are connected to the switching means of the CML circuit and how the first and second current lines, where the first current line according to embodiments of the invention may represent the logic output, are connected to the switching means of the CML circuitry. Another circuitry may be used for performing the XOR and the XNOR functions, again with 25   the resulting function being determined by how the input signals and their inverse signals are connected to the switching means of the CML circuit and how the first and second current lines are connected to said switching means. Thus, the third aspect of the present invention may also provide a converter for obtaining an analogue presentation of a logical bit-by-bit AND operation on the first digital signal 30   and a second digital signal.

According to an embodiment of the third aspect of the invention, the converter circuit may be designed for obtaining an analogue presentation of a bit by bit logic operation of the first digital signal and a second digital signal, said first and second

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digital signals having the same number of bits, wherein the CML circuits having a first logic input signal representing the value of a corresponding bit of the first digital signal are designed as first logic operating circuits, each said first logic operating circuit further having as input signal a second logic input signal representing a value

5 of a corresponding bit of the second digital signal, and said second logic input signal providing a second control signal for the switching between the first and the second conductive state. Here, each first logic operating circuit may be designed for performing a logic operation selected between the following logic operations: AND, NAND, OR, NOR, XOR or XNOR.

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For the converter circuit designed for a logic bit by bit operation, said first logic operating CML circuits may also have as input signals the inverse signals of the first and second logic input signals.

15 According to a preferred embodiment of the converter circuit designed for a logic bit by bit operation, the logic of the first logic operating circuits may be designed as first AND operating circuits, said AND operating circuits being designed so that in order for the first and second logic input signals to control the state of a CML circuit to be in the first conductive state, the corresponding bit values of the first digital signal and

20 the second digital signal shall both be active or logic high. Preferably, the switching means of a first AND operating CML circuit may comprise a first switch being controlled by the first logic signal, a second switch being controlled by the inverse of the first logic signal, a third switch being controlled by the second logic signal, and a fourth switch being controlled by the inverse of the second logic signal. The

25 switches may be arranged so that the CML circuit is in the first conductive state drawing or delivering current via the first current line through the first and third switches when the bit values corresponding to the first and second logic signals are both active, and so that the CML circuit is in the second conductive state drawing or delivering current via the second current line through the second and the third

30 switches when the bit value corresponding to the first logic signal is non-active and the bit value corresponding to the second logic signal is active, or through the fourth switch when the bit values corresponding to the first and second logic signals are both non-active.

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For the converter circuits designed for a logic bit by bit operation, it is preferred that the first and second logic signals being input to the same first logic operating CML circuit correspond to the same bit number of the first and the second digital signal, respectively.

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It should be understood that for the third aspect of the invention then by using the phrase that a signal is active is meant that the signal has a value, which may correspond to a logic high or 1, and by using the phrase that a signal is non-active is meant that the signal has a value, which may correspond to a logic low or zero.

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In the above discussion, an AND operating CML circuit according to an embodiment of the present invention has been discussed. However, as already mentioned the present invention also covers logic operations such as NAND, OR, NOR, XOR and XNOR.

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When the logic of the first logic operating circuits is designed as first NAND operating circuits, the NAND operating circuits should be designed so that in order for the first and second logic input signals to control the state of a CML circuit to be in the first conductive state, at least one of the corresponding bit values of the first digital signal and the second digital signal shall be non-active.

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When the logic of the first logic operating circuits is designed as first OR operating circuits, the OR operating circuits should be designed so that in order for the first and second logic input signals to control the state of a CML circuit to be in the first conductive state, at least one of the corresponding bit values of the first digital signal and the second digital signal shall be active.

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When the logic of the first logic operating circuits is designed as first NOR operating circuits, the NOR operating circuits should be designed so that in order for the first and second logic input signals to control the state of a CML circuit to be in the first conductive state, both of the corresponding bit values of the first digital signal and the second digital signal shall be non-active.

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When the logic of the first logic operating circuits is designed as first XOR operating circuits, the XOR operating circuits should be designed so that in order for the first and second logic input signals to control the state of a CML circuit to be in the first conductive state, one and only one of the corresponding bit values of the first digital

5   signal and the second digital signal shall be active.

When the logic of the first logic operating circuits is designed as first XNOR operating circuits, the XNOR operating circuits shall be designed so that in order for the first and second logic input signals to control the state of a CML circuit to be in

10   the first conductive state, both of the corresponding bit values of the first digital signal and the second digital signal shall be active or non-active.

According to an embodiment of the converter circuit designed for a logic bit by bit operation, said converter circuit may further be designed for obtaining an analogue

15   presentation of a bit by bit logic operation on a third and a fourth digital signal, said third and fourth digital signals having the same number of bits and having at least 2 bits. Here, the first, second, third and fourth digital signals may have the same number of bits. The converter circuit may further comprise a number of CML circuits being designed as second logic operating circuits, with each second logic operating

20   circuit having at least a first logic input signal representing the value of a corresponding bit of the third digital signal and a second logic input signal representing the value of a corresponding bit of the fourth digital signal, a third current line, a fourth current line and a constant current source, each of said second logic operating circuits further comprising means for switching the constant current

25   source between a first conductive state, in which the current source draws or delivers current via the third current line, and a second conductive state, in which the current source draws or delivers current via the fourth current line, said switching being controlled by at least said first and second logic input signals. It is preferred that the current drawn from or delivered to the first current lines of the first logic

30   operating circuits arranged in the modules is used for generating a first analogue output for the converter circuit, and that the current drawn from or delivered to the third current lines of the second logic operating circuits arranged in the modules is used for generating a second analogue output for the converter circuit.

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It should be understood that it is also within the third aspect of the invention that each second logic operating circuit may be designed as a logic operating circuit selected between the following logic operating circuits: AND, NAND, OR, NOR, XOR or XNOR logic operating circuit. It is however preferred that the first and the

5   second logic operating circuits are both designed for performing the same logic operation. It is also within a preferred embodiment that the second logic operating CML circuits further have as input signals the inverse signals of the first and second logic input signals.

10   According to an embodiment of a converter circuit having second logic operating circuits, the second logic operating circuits may be designed as second AND operating circuits, to thereby obtain an analogue presentation of a bit by bit AND operation of the third and the fourth digital signals. Here, the third and fourth digital signals may have P-bits, wherein for each bit m, where m is selected as an integer

15   larger than or equal to zero and smaller than or equal to P-1, there is a corresponding module m having at least one second AND operating circuit, with each second AND operating circuit of the module m having a first logic input signal representing the value of the corresponding bit m of the third digital signal and providing a first control signal for the switching between the first and the second

20   conductive state, and with each second AND operating circuit of the module m having a second logic input signal representing the value of the corresponding bit m of the fourth digital signal and providing a second control signal for the switching between the first and the second conductive state.

25   It is within an embodiment of the third aspect of the invention that the logic of said CML circuits being designed as second AND operating circuits is designed so that in order for the first and second logic input signals to control the state of a second AND operating circuit to be in the first conductive state, the corresponding bit values of the third digital signal and the fourth digital signal shall both be active. The switching

30   means of a second AND operating circuit may comprise a first switch being controlled by the first logic signal, a second switch being controlled by the inverse of the first logic signal, a third switch being controlled by the second logic signal, and a fourth switch being controlled by the inverse of the second logic signal. Here, the switches may be arranged so that the second AND operating circuit is in the first

conductive state drawing or delivering current via the third current line through the
first and third switches when the bit values corresponding to the first and second
logic input signals are both active, and so that the second AND operating circuit is in
the second conductive state drawing or delivering current via the fourth current line

5   through the second and the third switches when the bit value corresponding to the
first logic signal is non-active and the bit value corresponding to the second logic
signal is active, or through the fourth switch when the bit values corresponding to
the first and second logic input signals are both non-active.

10   For the converter circuits having second logic operating circuits, the first and second
logic signals being input to the same second logic operating circuit may correspond
to the same bit number of the third and the fourth digital signals, respectively. It is
within an embodiment of the invention that the third and fourth digital signals are the
inverse signals of the first and second digital signals, respectively, or the inverse

15   signals of the second or first digital signals, respectively.

For converter circuits having modules with first logic operating circuits and modules
with second logic operating circuits, and wherein there for each module k is one
corresponding first logic operating circuit, then it is preferred that for each module m,

20   there is one corresponding second logic operating circuit.

For converter circuits having modules with first logic operating circuits and modules
with second logic operating circuits, and wherein there for each module k are 2^k
corresponding first logic operating circuit, then it is preferred that for each module m,

25   there are 2^m corresponding second AND operating circuits.

In the above discussion, a second AND operating CML circuit according to an
embodiment of the present invention has been discussed. As already mentioned the
present invention also covers embodiments in which the second logic operating

30   circuit performs logic operations such as NAND, OR, NOR, XOR and XNOR. Here,
the second logic operating circuit may be designed in line with the discussion of the
first logic operating circuit, when the first logic operating circuit is designed as a
NAND, OR, NOR, XOR or XNOR operating circuit. However, the second logic
operating circuits have input signals representing a value of a corresponding bit of

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the third and fourth digital signals, and the current is delivered or drawn by the
constant current source from the third or fourth current lines.

It has been discussed above that the converter circuit of the present invention may
comprise first and second logic operating circuits for obtaining an analogue
presentation of a bit by bit logic operation of a first and a second digital signal, and
an analogue presentation of a bit by bit logic operation of a third and a fourth digital
signal.

According to another embodiment of the third aspect of the invention, there is
provided a converter circuit being designed for obtaining an analogue presentation
of a bit by bit first logic operation on the first digital signal and a second digital
signal, and for obtaining an analogue presentation of a bit by bit first logic operation
of the inverse signals of the first and second digital signals, said first and second
digital signals having the same number of bits. Here, the CML circuits having a first
logic input signal representing the value of a corresponding bit of the first digital
signal may be designed as combined logic operating circuits, each combined logic
operating circuit further having:
a second logic input signal representing a value of a corresponding bit of the second
digital signal, and a third current line;
said switching means further being adapted for switching the constant current
source between the first conductive state, in which the current source draws or
delivers current via the first current line, the second conductive state, in which the
current source draws or delivers current via the second current line, and a third
conductive state in which the current source draws or delivers current via the third
current line; and
said first and second logic input signals providing corresponding first and second
control signals for the switching between the first, second and third conductive
states.

The above described converter circuit design having combined logic operating
circuits may have a corresponding design in accordance with an aspect of the
present invention, which may also be used for digital input signals having only one
bit. Thus, according to a fourth aspect of the present invention there is provided a

converter circuit for obtaining an analogue presentation of a bit by bit first logic
operation on a first digital signal and a second digital signal, and for obtaining an
analogue presentation of a bit by bit first logic operation of the inverse signals of the
first and second digital signals, said first and second digital signals having the same

5   number of bits, said circuit comprising:
a number of current mode logic circuits, CML circuits, being designed as combined
logic operating circuits, with each combined logic operating circuit having a first logic
input signal representing the value of a corresponding bit of the first digital signal
and a second logic input signal representing a value of a corresponding bit of the

10   second digital signal, a first current line, a second current line, a third current line
and a constant current source, each of said combined logic operating circuits further
having means for switching the constant current source between a first conductive
state, in which the current source draws or delivers current via the first current line, a
second conductive state, in which the current source draws or delivers current via

15   the second current line, and a third conductive state in which the current source
draws or delivers current via the third current line; and
said first and second logic input signals providing corresponding first and second
control signals for the switching between the first, second and third conductive
states.

20

For converter circuits having one or more combined logic operating circuits, it is
preferred that the current drawn from or delivered to the first current lines of the
combined logic operating circuits arranged in the modules is used for generating a
first analogue output for the converter circuit, and that the current drawn from or

25   delivered to the third current lines of the combined logic operating circuits arranged
in the modules is used for generating a second analogue output for the converter
circuit. The converter circuit may be designed so that the first logic operation is
selected between the following logic operations: AND, NAND, OR, NOR, XOR or
XNOR logic operating circuit.

30

It is preferred that each combined logic operating circuit is designed as a combined
AND operating circuit, to thereby obtain an analogue presentation of a bit by bit AND
operation on the first digital signal and the second digital signal, and for obtaining an

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analogue presentation of a bit by bit AND operation of the inverse signals of the first and second digital signals.

For converter circuits having one or more combined logic operating circuits, each combined logic operating circuit may further have a third logic input signal representing the inverse value of the bit corresponding to the first digital signal, and a fourth logic input signal representing the inverse value of the bit corresponding to the second digital signal, said third and fourth logic input signals providing corresponding third and fourth control signals for the switching between the first, second and third conductive states.

According to a preferred embodiment of a converter circuit having the combined logic operating circuits designed as AND operating circuits, the logic of the combined AND operating CML circuits is designed so that in order for the logic input signals to control the state of a combined AND operating circuit to be in:
the first conductive state, the corresponding bit values of the first digital signal and the second digital signal shall both be active;
the third conductive state, the corresponding bit values of the first digital signal and the second digital signal shall both be non-active; and
the second conductive state, the corresponding bit value of the first digital signal shall be non-active with the corresponding bit value of the second digital signal being active, or the corresponding bit value of the first digital signal shall be active with the corresponding bit value of the second digital signal being non-active.

For converter circuits having one or more combined logic operating circuits, it is preferred that the first and second logic input signals correspond to the same bit number of the first and second digital signals, respectively.

According to an embodiment of the converter circuits having one or more combined logic operating circuits, the switching means of the combined AND operating circuit comprises a first switch being controlled by the first logic signal, a second switch being controlled by the third logic signal or the inverse of the first logic signal, a third switch being controlled by the second logic signal, a fourth switch being controlled by the fourth logic signal or the inverse of the second logic signal, a fifth switch

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being controlled by the third logic signal of the inverse of the first logic signal, and a sixth switch being controlled by the first logic signal. Here, the switches may be arranged so that the combined AND operating circuit is in:

the first conductive state drawing or delivering current via the first current line

5   through the first and third switches when the bit values corresponding to the first and second logic signals are both active;

the third conductive state drawing or delivering current via the third current line through the fifth and fourth switches when the bit values corresponding to the first and second logic signals are both non-active;

10   the second conductive state drawing or delivering current via the second current line through the third and second switches when the bit value corresponding to the first logic signal is non-active and the bit value corresponding to the second logic signal is active; and

the second conductive state drawing or delivering current via the second current line

15   through the sixth and fourth switches when the bit value corresponding to the first logic signal is active and the bit value corresponding to the second logic signal is non-active.

In the above discussed embodiments of the third and fourth aspects of the invention,

20   examples have been given on a converter circuit being designed for obtaining an analogue presentation of a bit by bit first logic operation of a first and a second digital signal, and for obtaining an analogue presentation of a bit by bit first logic operation of the inverse signals of the first and second digital signals. Also here, when using a complementary logic having both the truth and the inverse values of a

25   signal as input to the logic circuit, the circuitry used for performing first logic operations being AND, NAND, OR or NOR functions is very much the same, the resulting function being determined by how the input signals and their inverse signals and the first, second and third current lines are all connected to the switching means of the CML circuit. Here, the current in the first current line according to

30   embodiments of the invention may be used for the first analogue output and the current in the third current line may be used for the second analogue output. Another circuitry may be used for the first logic operations to perform XOR and XNOR functions, again with the resulting function being determined by how the input signals and their inverse signals are connected to the switching means of the

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CML circuit and how the first, second and third current lines are connected to said switching means.

It should be understood that for the herein described bit by bit first logic operations
5   of the first and second digital signals and the inverse of these signals, then if it is desired to use a signal being the inverse of the second signal, then a bit by bit first logic operation of the first signal and the inverse of the second signal can be obtained, when using complementary logic by shifting the truth logic input signals of the second signal from the truth to the inverse signals, and by shifting the inverse
10 logic input signals of the second signal from the inverse to the truth signal.

It is preferred that for the converter circuits of the third and fourth aspects of the invention, the number of CML circuits are being powered by the same power supply having a positive supply terminal and a negative or ground terminal. It is also
15 preferred that the constant current sources of each of the CML circuits of said modules or each of the CML circuits are designed to draw or deliver substantially the same current.

For a converter circuit according to the third or fourth aspect of the invention having
20 modules with CML circuits, and wherein for each module corresponding to bit k there are 2^k corresponding CML circuits having a first current line and a second current line, it is preferred that each said first current line is supplied from the same, first supply line. Here, the current drawn from or delivered to said first supply line by the first current lines may represent a first analogue output signal for the converter
25 circuit.

For a converter circuit according to the third or fourth aspect of the invention having modules with combined logic operating CML circuits, and wherein for each module corresponding to bit k there are 2^k corresponding combined logic operating circuits
30 having a first current line, a second current line and a third current line, it is preferred that each said first current line is supplied from the same, first supply line, and each said third current line is supplied from the same, third supply line. Here, the current drawn from or delivered to said first supply line by the first current lines may represent a first analogue output signal for the converter circuit, and the current

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drawn from or delivered to said third supply line by the third current lines may represent a second analogue output signal for the converter circuit.

5   For a converter circuit according to the third aspect of the invention having modules with second logic operating CML circuits, and wherein for each module corresponding to bit m there are 2^m corresponding CML circuits having a third current line and a fourth current line, it is preferred that each said third current line is supplied from the same, third supply line. Here, the current drawn from or delivered to said third supply line by the third current lines may represent a second analogue

10   output signal for the converter circuit.

          For a converter circuit according to the third or fourth aspect of the invention having modules with CML circuits, and wherein for each module corresponding to bit k there is one corresponding CML circuit having a first current line and a second

15   current line, it is preferred that each said first current line is supplied from the same power supply via a first resistor network or via a first capacitor network having a first voltage output representing a first analogue output signal for the converter circuit.

          For a converter circuit according to the third or fourth aspect of the invention having

20   modules with combined logic operating CML circuits, and wherein for each module corresponding to bit k there is one corresponding combined logic operating circuit having a first current line, a second current line and a third current line, it is preferred that each said first current line is supplied from the same power supply via a first resistor network or via a first capacitor network having a first voltage output

25   representing a first analogue output signal for the converter circuit, and that each said third current line is supplied from said power supply via a second resistor network or via a second capacitor network having a second voltage output representing a second analogue output signal for the converter circuit.

30   For a converter circuit according to the third aspect of the invention having modules with second logic operating CML circuits, and wherein for each module corresponding to bit m there is one corresponding CML circuit having a third current line and a fourth current line, it is preferred that each said third current line is supplied from the same power supply via a second resistor network or via a second

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capacitor network having a second voltage output representing a second analogue output signal for the converter circuit.

For a converter circuit according to the third or fourth aspect of the invention having a first resistor network, it is preferred that the first resistor network is formed as a first R −2R network having the first voltage output. For a converter circuit according to the third or fourth aspect of the invention having a second resistor network, it is preferred that the second resistor network is formed as a second R −2R network having the second voltage output.

According to an embodiment of the third or fourth aspect of the invention, the second current lines of the CML circuits are powered by the positive terminal of a common power supply or via a resistor connected to the positive terminal of the power supply. For converter circuits having second logic operating circuits, it is preferred that the fourth current lines of the second logic operating CML circuits are powered by the positive terminal of the power supply or via a resistor connected to the positive terminal of the power supply. Preferably, the second current lines and the fourth current lines of the CML circuits are powered from the same supply line.

According to an embodiment of the third or fourth aspect of the invention, the constant current sources of the CML circuits are delivering current to the negative or ground terminal of a common power supply.

According to a preferred embodiment of the third or fourth aspect of the invention, the switching means of the CML circuits is made using N-MOS technology. However, the present invention also covers converter circuits wherein the switching means of the CML circuits is made using P-MOS technology or other technologies, in which it is possible to implement a switch function e.q. (Bipoar, METFET etc.)

It should be understood that some of the embodiments of the converter circuits of the third and fourth aspects of the present invention may be used for the phase comparator according to the first and second aspects of the invention.

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Thus, the present invention also covers a phase-locked loop according to the first
aspect of the invention and having a phase comparator including a converter circuit,
and the present invention further covers a phase comparator according to the
second aspect of the invention including a converter circuit, wherein the converter

5   circuit of the phase comparator comprises first AND operating circuits and second
AND operating circuits for performing said first and second logic bit by bit operation,
respectively, said first and second AND operating circuits being selected from
converter circuits of the third aspect of the invention having both first and second
AND operating circuits. Here, the output of the first accumulator is the first digital

10   signal, the inverted output of the second accumulator is the second digital signal, the
inverted output of the first accumulator is the third digital signal, and the output of
the second accumulator is the fourth digital signal.

The present invention also covers a phase-locked loop according to the first aspect

15   of the invention having a phase comparator including a converter circuit, and the
present invention further covers a phase comparator according to the second aspect
of the invention including a converter circuit, wherein the converter circuit of the
phase comparator comprises combined AND operating circuits for performing said
first and second logic bit by bit operation, said combined AND operating circuits

20   being selected from converter circuits of the third or fourth aspect of the invention
having combined AND operating circuits. Here, the output of the first accumulator is
the first digital signal, and the inverted output of the second accumulator is the
second digital signal.

25   In a conventional phase-locked loop as shown in Fig. 1, the output signal of the
VCO 101 is divided by integers N_F and N_R, while the reference clock signal is
divided by the integer N_V, to thereby obtain that the phase comparator receives two
signals having the same frequency.

30   I is also possible to obtain input signals for the phase comparator having the same
frequency, if the reference clock signal is multiplied by an integer N_V, and the output
signal divided by N_F is further multiplied by an integer N_V. This is illustrated in Fig. 5
and is used for the design of the phase-locked loop of the present invention.

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According to the present invention the multiplication of the reference signal or clock
by N_R is obtained by accumulating a first predefined phase step N_R to a first
accumulated phase value in response to the frequency of the reference signal, and
the multiplication of the VCO signal or the divided VCO signal by N_V is obtained by
5   accumulating a second predefined phase step N_V to a second accumulated phase
value in response to the frequency of the obtained VCO signal.

However, the analysis used for the conventional phase-locked loop and the phase-
locked loop of the present invention is the same and is giving in the following.

10

Constructing a phase-locked loop of the present invention as described above have
a number of benefits. These benefits may most easily be seen from an analysis of
the circuit function. Starting with analysing the above mentioned phase-locked loop
in an ideal non-digital case, the phase versus time of the output signal and the
15   reference signal may be represented as

$$\phi_R(t) = \omega_R t + \phi_{R0}$$
$$\phi_V(t) = \omega_V t + \phi_{V0} \qquad\qquad [1]$$

where index R is the reference and index V is the variable frequency.
20   The period time T_R and T_V of the signal may be calculated as

$$T_R = \frac{2\pi}{\omega_R} \quad and \quad T_V = \frac{2\pi}{\omega_V} \qquad\qquad [2]$$

The fractional relationship between T_R and T_V as
25

$$T_R = N_R \Delta t, \qquad \tfrac{1}{2} N_R \in \mathcal{N}$$
$$T_V = N_V \Delta t, \qquad \tfrac{1}{2} N_V \in \mathcal{N} \qquad\qquad [3]$$

where N_R and N_V are the predetermined phase step values corresponding to the
integer numbers by which the frequencies are multiplied.
30

From [1], [2] and [3] the following relation may be defined as

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$$N_R \phi_R(t) = \frac{2\pi}{N_R \Delta t} N_R t + N_R \phi_{R0}$$

$$N_V \phi_V(t) = \frac{2\pi}{N_V \Delta t} N_V t + N_V \phi_{V0} \qquad [4]$$

The phase error may be defined as

$$2\pi \cdot e(t) = \epsilon(t) = N_R \phi_R(t) - N_V \phi_V(t) \qquad [5]$$

If the relations in [3] and [4] are fulfilled, the slope of the phase functions may be derived as $N_R \Phi_R(t)$ and $N_V \Phi_V(t)$, where both of the slopes are equal to $K_\Phi = 2\pi/\Delta t$. This leads to the following error relation

$$\epsilon(t)\Big|_{\frac{\omega_R}{\omega_V} = \frac{N_V}{N_R}} = N_R \phi_{R0} - N_V \phi_{V0} \qquad [6]$$

This means that the phase error function is equal to the traditional PLL when $\omega_R/\omega_V = N_V/N_R$. When $N_R = N_V$, the phase error is exactly the same as a traditional PLL. Laplace transforming [4], the spectral domain becomes

$$\mathcal{P}_R(s) = \mathcal{L}\{\frac{N_R}{2\pi}\phi_R(t)\} = \frac{N_R \omega_R}{2\pi s^2} + \frac{N_R}{2\pi}\phi_R = \frac{N_R}{T_R s^2} + \frac{N_R}{2\pi}\phi_R$$

$$\mathcal{P}_V(s) = \mathcal{L}\{\frac{N_V}{2\pi}\phi_V(t)\} = \frac{N_V \omega_V}{2\pi s^2} + \frac{N_V}{2\pi}\phi_V = \frac{N_V}{T_V s^2} + \frac{N_V}{2\pi}\phi_V \qquad [7]$$

In the ideal case, the phase function of the PLL is a straight line with a slope. In the digital implementation of a PLL, the phase function becomes a staircase function. This corresponds to an error function between the straight line and the staircase which is a sawtooth function. From [4] the staircase phase function may be defined as

$$R(t)\Big|_{t=T_R i} = \frac{N_R}{2\pi}\phi_R(t)\Big|_{t=T_R i} \qquad i \in \mathcal{N}^0$$

$$V(t)\Big|_{t=T_V i} = \frac{N_V}{2\pi}\phi_V(t)\Big|_{t=T_V j} \qquad j \in \mathcal{N}^0 \qquad [8]$$

which in the continuous time domain gives the staircase phase function as

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$$R(t)\Big|_{t\in]T_R i-\frac{T_R}{2}:T_R(i+1)\frac{T_R}{2}]} = (\frac{N_R}{T_R}\Delta t)i + \frac{N_R}{2} + N_R\frac{\phi_{R0}}{2\pi} \qquad i\in\mathcal{N}^0$$

$$V(t)\Big|_{t\in]T_V j-\frac{T_V}{2}:T_V(j+1)\frac{T_V}{2}]} = (\frac{N_V}{T_V}\Delta t)j + \frac{N_V}{2} + N_V\frac{\phi_{V0}}{2\pi} \qquad j\in\mathcal{N}^0 \tag{9}$$

and which in the spectral domain may be written as

$$\mathcal{L}\{R(t)\} = \mathcal{R}(s) = \frac{N_R}{s(1-e^{-T_R s})}e^{-\frac{T_R}{2}s} + \frac{N_R}{2} + \frac{N_R}{2\pi}\phi_{R0}$$

$$\mathcal{L}\{V(t)\} = \mathcal{V}(s) = \frac{N_V}{s(1-e^{-T_V s})}e^{-\frac{T_R}{2}s} + \frac{N_V}{2} + \frac{N_V}{2\pi}\phi_{V0} \tag{10}$$

$$\mathcal{R}(s) = \left\{\frac{N_R}{s(1-e^{-T_R s})}e^{-\frac{T_R}{2}s} - \frac{N_R}{T_R s^2} + \frac{N_R}{2}\right\} + \frac{N_R}{T_R s^2} + \frac{N_R}{2\pi}\phi_{R0}$$

$$\mathcal{V}(s) = \left\{\frac{N_V}{s(1-e^{-T_V s})}e^{-\frac{T_V}{2}s} - \frac{N_V}{T_V s^2} + \frac{N_V}{2}\right\} + \frac{N_V}{T_V s^2} + \frac{N_V}{2\pi}\phi_{V0} \tag{11}$$

From [7] and [11] the following relation may be defined as

$$\mathcal{R}(s) = \mathcal{S}_\mathcal{R}(s) + \mathcal{P}_\mathcal{R}(s)$$

$$\mathcal{V}(s) = \mathcal{S}_\mathcal{V}(s) + \mathcal{P}_\mathcal{V}(s) \tag{12}$$

From [11] and [12] the time domain functions for S_R and S_V may be derived as

$$S_R(t)\Big|_{t\geq 0} = \mathcal{L}^{-1}\{\mathcal{S}_\mathcal{R}(s)\} = -\frac{N_R}{\pi}\sum_{k\in\mathcal{N}^0}(-1)^k\frac{\sin((2k+1)\omega_{S_V}t)}{2k+1}$$

$$S_V(t)\Big|_{t\geq 0} = \mathcal{L}^{-1}\{\mathcal{S}_\mathcal{V}(s)\} = -\frac{N_V}{\pi}\sum_{k\in\mathcal{N}^0}(-1)^k\frac{\sin((2k+1)\omega_V t)}{2k+1} \tag{13}$$

The phase error function from [5] may be derived in a similar manner as

$$E(t) = R(t) - V(t) = e(t) + S_R(t) - S_V(t) \tag{14}$$

where the only difference between the two functions is the sawtooth function given by [13], which in the spectral domain becomes

$$\mathcal{E}(s) = \mathcal{R}(s) - \mathcal{V}(s) \tag{15}$$

Analysing the staircase error function, it appears that there are no spectral harmonics below ω_R or ω_V. This means that there are no sub-harmonics of the reference signal nor the variable signal.

5   From the above the selected output frequency becomes a function of the reference frequency and the integers by which the frequencies are multiplied as

$$f_O = (N_R/N_V)\, N_F f_R \qquad [16]$$

10   According to [13] the generated spurious may be selected to be as far apart as desired by selecting the two integers N_R and N_V appropriately, because it is their ratio that selects the output frequency. Also, according to [13], the amplitude of the spurious decreases the further away from the base frequency they are. This provides a large loop-bandwidth, which means a fast lock-in time. It is therefore both

15   possible to select the bandwidth of the loop and how closely the spurious are placed, thereby producing a component which is more like the ideal phase-locked loop, without some of the disadvantages due to the way the component is constructed. The phase-locked loop is also easily constructed with standard "of-the-shelf" components.

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Other features and advantages of the method of the present invention will become apparent from the following description of preferred embodiments, taken in conjunction with the accompanying drawings.

25   BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an example of a phase-locked loop according to the prior art,

Fig. 2 is a first embodiment of a phase comparator or frequency comparator

30   according to the invention,

Fig. 3 is a second embodiment of a phase comparator or frequency comparator according to the invention,

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Fig. 4 is a third embodiment of a phase comparator or frequency comparator according to the invention,

Fig. 5 illustrates a phase-locked loop according to the invention,

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Fig. 6 shows two blocks with each block having a first one-bit combined logic digital-to-analogue converter according to the invention,

Fig. 7 shows one block of a second combined logic digital-to-analogue converter

10   according to the invention performing the same function as the two blocks of Fig. 6,

Fig. 8 shows a circuit example for a combined logic digital-to-analogue converter according to the converter of Fig. 7,

15   Fig. 9 shows another circuit example for a combined logic digital-to-analogue converter according to the converter of Fig. 7,

Fig. 10 shows a circuit example of a 4-bit combined logic digital-to-analogue converter according to the invention using a resistor network,

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Fig. 11 shows another circuit example of a 4-bit combined logic digital-to-analogue converter according to the invention using constant current sources,

Fig. 12 shows a combination of the 4-bit converter of Fig. 10 using a resistor

25   network and a 4 bit combined logic digital-to-analogue converter of the invention using a capacitor network,

Fig. 13 shows an example of a loop filter using the circuit of Fig. 10, and

30   Fig. 14 shows an example of a loop filter using the circuit of Fig. 11.

DESCRIPTION OF PREFERRED EMBODIMENTS

In the figures are all lines with a small line across representing a binary number.

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Fig. 1 is an example of a phase-locked loop according to the prior art. The phase-
locked loop 100 includes a voltage controlled oscillator 101, a frequency divider 102,
and a phase comparator 103. The voltage controlled oscillator or VCO 101 includes
a frequency controlling input terminal and an output terminal. As shown in Fig. 1, the
5   output terminal of the VCO 101 is operatively connected to an input terminal of the
frequency divider 102. Further, the frequency divider 102 includes an output terminal
which is operatively connected to a first input terminal of the phase comparator 103.
The phase comparator 103, which is also denoted a phase detector 103 in the
following, also includes a second input terminal and an output terminal. The output
10   terminal of the phase detector 103 is operatively connected to the input terminal of
the VCO 101. Hereby the voltage controlled oscillator 101, the frequency divider
102, and the phase comparator 103 form a closed loop.

The voltage controlled oscillator or VCO 101 is adapted for retrieving an control
15   signal via the input terminal of the VCO and for generating an oscillating electrical
output signal having a frequency which is determined by the control signal. The
frequency divider 102 is adapted for dividing the frequency of a signal supplied
thereto, i.e. the output signal of the VCO 101, and hereby generating a signal having
a reduced frequency compared to the frequency of the input signal supplied thereto.
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The phase comparator 103 is adapted for deriving a control signal from the
frequency-divided output signal and a reference signal supplied thereto via the first
and the second input terminal, respectively. Hereby, when the phase comparator
103 is supplied by the frequency-divided output signal from the VCO 101 and the
25   reference signal, an output signal reflecting the phase error between the two input
signals is generated. For example, the phase comparator may output a voltage
proportional to the phase difference between the input signals. As mentioned above,
the phase comparator 103 is coupled to the voltage controlled oscillator 101, i.e.
during operation the control signal generated by the phase comparator 103 is
30   supplied to the VCO 101 via the frequency control input terminal of said voltage
controlled oscillator.

The shown phase-locked loop also includes a loop filter 105 adapted for
smoothening the output of phase detector 103, i.e. filtering the signal used to control

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the voltage controlled oscillator 101 and hereby reducing unwanted spurious occurring in the signal. Further, as illustrated in Fig. 1, the frequency divider 102 may include one or more frequency dividing parts 102A, 102B. Hereby, a first frequency dividing part 102A and a second frequency dividing part 102B may be adapted for performing the frequency division in two successive steps. In addition, the reference signal may also be derived from another signal, e.g. the reference signal may be an output signal of a frequency divider 109 as shown in Fig. 1.

In short the operation of a phase-locked loop may be explained as follows. During operation the frequency divider 102 receives an oscillating input signal from the VCO and generates an oscillating signal having a reduced frequency. The phase detector 103 outputs a signal, which is determined by the phase difference between the two input signals supplied thereto, ie. the phase difference between the output signal of the frequency divider 102 and the reference signal. When the phase of the output signal from the frequency divider 102 lags behind of the phase of the reference signal, the phase detector outputs an "up" signal, e.g. by increasing the output voltage which is supplied to the VCO 101 via the loop filter 105. On the other hand, when the phase of the output signal from the frequency divider 102 leads that of the reference signal, the phase detector outputs a "down" signal, e.g. by decreasing the output voltage which is supplied to the VCO 101 via the loop filter 105. The voltage controlled oscillator 101 outputs an oscillating signal determined by the output voltage from the loop filter 105. Hereby, the frequency of the VCO output signal increases and decreases when the phase detector 103 outputs an "up" and a "down" signal, respectively. As a result the phase difference between output signal of the frequency divider 102 and the reference signal is decreased. When the phase-locked loop 100 is in a phase-locked state, the phase of the output signal of the frequency divider 102 is in alignment with that of the reference signal and the frequency of the two signals are the same. There are therefor three signals of importance in the phase-locked loop: A_0, A_V and A_R, which are cyclic functions and may be described as

$$A_0(t) = \sin(\omega_0 t + \phi_0)$$
$$A_R(t) = \sin(\omega_R t + \phi_{R0}) = \sin(\phi_R(t))$$
$$A_V(t) = \sin(\omega_V t + \phi_{V0}) = \sin(\phi_V(t))$$

[17]

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When the system is in lock the following condition is fulfilled

$$\omega_D = \frac{\omega_R}{N_V} = \frac{\omega_V}{N_R} = \frac{\omega_0}{N_R \cdot N_F}$$

[18]

5   which gives a phase error

$$\phi_D(t) = \frac{\phi_R(t)}{N_V} - \frac{\phi_V(t)}{N_R}$$

[19]

The effective angle frequency by which the phase comparator operates is that which
10   corresponds to ω_D. This will lead to the generation of spurious, because this angle
frequency is slower than ω_0. The spurious are unwanted, because they will cause
unwanted channels to interfere and must be filtered out by a filter placed in the loop.
However, this reduces the bandwidth of the phase-locked loop.

15   Example of a conventional PLL:

Here we want to design a channel selector by using a traditional PLL structure with
channels from 2400MHz to 2480MHz and with a channel step of 1MHz.
The maximum angle frequency is $\omega_D=2\pi 1MHz$, and because of this we are limited to
20   chose the reference frequency to an integer number N_V times 1MHz.
We can chose $N_V=19$ this means that the reference frequency is 19MHz.
We set $N_F=1$. The channel can be selected by changing the value of N_R from
2400,2401,2402 until 2480.

25   Example of a PLL according to the present invention:

Here we chose to divide the output of the VCO with the integer number $N_F=32$
because it is easy to implement a high speed divide by 32 in hardware, and we have
a given reference frequency of $f_R=18.6MHz$. We can from this calculate the relation
30   between the predetermined phase values N_V and N_R from equation [16]. Here N_R is
first predetermined phase step value used for the reference signal and N_V is the
second predetermined phase value used for divided output signal.

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We want channels from 2400MHz to 2480MHz with channel steps of 1MHz. So by
setting the output frequency $f_O = (2400 + M)$ MHz, where M is the channel number,
we obtain from equation [16] $(2400+M)$ MHz $= (N_R/ N_V)N_F f_R$.
From here we can the chose the relation between N_V and N_R, and for $N_V=2976$, we

5   get that $N_R=12000+5M$.

Fig. 2 illustrates a first embodiment of a phase comparator or frequency comparator
according to the invention. The phase comparator includes a first accumulator 201,
a second accumulator 202 and subtracting means 203. The first accumulator 201

10   and the second accumulator 202 both include an input terminal and an output
terminal. The first and the second accumulator 201, 202 are operatively connected
to a first and a second input terminal of the subtracting means 203. The first and the
second accumulator 201, 202 are both adapted for receiving an input signal via the
input terminal and generating an output signal, which is supplied to the subtracting

15   means. Responsive to the input signal received via the input terminal of the
accumulator 201, the first accumulator 201 is adapted for accumulating a first value
in a register or memory thereof. Likewise, responsive to the input signal received via
the input terminal of the accumulator 202, the second accumulator 202 is adapted
for accumulating a second value in a register or memory thereof. The phase

20   comparator is adapted for supplying the first and the second accumulated values to
the subtraction means 203 and thereby the difference there between may be
determined. When the first and the second accumulator 201, 202 are adapted for
being triggered by trigger signals reflecting the phase of a first and a second signal,
respectively, the difference between the accumulated values reflects the phase

25   difference between the first and the second signal.

In the shown embodiment, the first accumulator 201 includes a first digital register
208, a second digital register 209, a first adder 210 and a first trigger 205. The first
adder 201 is adapted for being supplied with the contents of the two registers 208,

30   209 or at least a subset thereof, e.g. a number of the least significant bits, as input
values. The first adder 210 is adapted for adding the values supplied as input and
hereby generating a digital output signal. The output of the adder 210 is connected
to the input of the first register 208 which is adapted for being trigged by a trigger
signal supplied thereto via the first trigger 205 connected thereto. When the first

register 208 is trigged, the input value supplied thereto by the adder 210 written into the first register 208 and hereby saved as the new updated content thereof. For simplicity, in the shown embodiment the contents of the registers 208 and 209 are continuously present at the output terminals. As a result the output of the first adder

5   210 is present at the input terminal of the register 208 and therefore the content is updated when the register 208 is trigged by trigger means 205.

When the second register 209 holds a predefined phase step value, the first register 208 includes a first accumulated phase value, which is updated when trigged. A first

10   oscillating signal $A_R(t)$, e.g. a reference signal, may be supplied as input to the first trigger means 205 and hereby the first trigger means 205 forms a trigger signal which is supplied to the first register 208. As indicated in Fig. 2, the first trigger means 205 is adapted for trigging the first register 208 when a first input signal supplied thereto exceeds a first predetermined level, i.e. the first accumulator 201 is

15   adapted for, responsive to a reoccurring event in a first oscillating signal supplied thereto, adding a first predefined phase step value to a first accumulated phase value.

In the shown embodiment, the second accumulator 202 is implemented similarly to

20   the above-mentioned implementation of the first accumulator 201, and includes two registers 211, 212, a second adder 213, and a second trigger 206. The output of the second trigger 206 is connected to a trigger input of a first of the two registers. A second oscillating signal $A_V(t)$, e.g. a frequency-divided version of an voltage controlled oscillator output signal, may be supplied as an input to the second trigger

25   206. As indicated, the second trigger 206 is adapted for trigging the first of the two registers 211 when a second input signal supplied thereto exceeds a second predetermined signal level, i.e. the second accumulator 202 is adapted for, responsive to a reoccurring event in the second oscillating signal supplied thereto, adding a second predefined phase step value to a second accumulated phase

30   value. When the first of the two registers is trigged the output of the second adder 213, i.e. the sum of the contents of the two registers 211, 212, is stored as the new content of the register 211.

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When a first and a second oscillating signal are supplied to the first and the second trigger means 205, 206, respectively, and when the second and the fourth registers 209, 212 are given value representing predefined phase steps, the outputs of the first and the second accumulator are accumulated phase values reflecting the phase

5   of the first and the second oscillating signal, respectively. The subtracting means 203 is adapted for subtracting the first accumulated phase value and the second accumulated phase value and hereby determining the phase error between the first and the second signal supplied to the trigger means 205, 206. As illustrated in Fig. 2, the output of the subtracting means 203 is connected to a digital-to-analogue

10   converter 204 adapted for converting the digital representation of the phase error to an analogue value and hereby forming and analogue output signal of the phase comparator.

The above-mentioned embodiment is advantageous due to the simplicity, which is

15   obtained due to the calculation of the phase error as a digital subtraction. The price, on the other hand, is that the digital subtraction may generate spikes and hazards in the resulting phase error signal. In the following a second embodiment of a phase comparator according to the invention is described. This embodiment is an example of a phase comparator which is both simple and hereby easy to implement, and in

20   which spikes and hazards do not occur in the resulting output signal.

Fig. 3 illustrates a second embodiment of a phase comparator according to the invention. In this embodiment, the first and the second accumulator 201, 202 is implemented as described in relation to Fig. 2. Therefore the first and the second

25   accumulator 201, 202 and the function thereof will not be described further below.

In contrast to the embodiment shown in Fig. 2, the output of the first and the second accumulators 201, 202 in the embodiment shown in Fig. 3 are connected to a first and a second digital-to-analogue converter 204A, 204B, respectively. Hereby, when

30   a digital value representing an accumulated phase value is supplied the first and the second digital-to-analogue converter 204A, 204B, respectively, an analogue representation thereof is formed. The output of the first and second digital-to-analogue converter 204A, 204B are connected to a subtraction means 223 which is

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adapted for performing an analogue subtraction and hereby forming an analogue output signal of the phase comparator.

Optionally the phase comparator may include a first and a second AND-gate 220, 221 as illustrated in Fig. 3. In the shown embodiment, the output of the first accumulator 201 and the second accumulator 202 is connected to a non-inverted and an inverted input of the first AND-gate 220, respectively. Further, the output of the first accumulator 201 and the second accumulator 202 is connected to an inverted and a non-inverted input of the second AND-gate 221, respectively. As illustrated in Fig. 3, the AND-gates 220, 221 are adapted for performing a bit-by-bit AND operation on the digital signals supplied thereto.

Using AND-gates as described above, the subtraction of the two digital numbers is pre-processed. By further digital-to-analogue converting the digital numbers with the two digital-to-analogue converters 204A, 204B and performing the subtraction by using analogue subtraction means 223, the risk of ripples are significantly minimised.

The analogue subtraction means in the above-mentioned phase comparator is advantageous as no spikes or hazards will occur in the resulting output signal due to short lived error signals on the higher bits. Therefore, this embodiment has been found very useful.

The two adding means 210 and 213 does not contribute to a similar problem as described above. This is because the output from the two adding means 210 and 213 are only read into said first digital register 208 and said second digital register 209 when they are triggered by said first trigger 205 or said second trigger 206. The outputs from said two adding means 210 and 213 therefore have adequate time to settle to stable outputs.

Fig. 4 illustrates a third embodiment of a phase comparator according to the invention. The shown embodiment includes a synchronous reset of the most significant bit (MSB) of the first register 208 and the third register 211, i.e. the registers adapted for including accumulated values. It is, however, not the absolute

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value of the digital number in the registers, but the difference between the numbers.
The synchronous reset may be implemented as illustrated in Fig. 4. In the shown
embodiment the first register 208 and the third register 211 have the same length,
i.e. the two registers include the same number of bits. When the phase comparator

5   is in use the contents of the two registers are accumulated as a result of the above-
mentioned trigger signal supplied thereto. As the difference between the contents of
the two registers is calculated, it has to be insured that a possible overflow of the
registers is taken care of. This is due to the fact that an uncontrolled overflow may
otherwise lead to an undesired result when performing the subsequent subtraction.

10   To overcome this problem an AND-gate 404 is connected to the first and the third
register 208, 211. The AND-gate 404 is adapted for being supplied with the most
significant bit (MSB) of the first register 208 and the third register 211 as shown in
Fig. 4. The output of the AND-gate 404 is connected to a reset input of both the first
register 208 and the third register 211. Hereby, when the most significant bit of both

15   the first and the third register 208, 211 is "1", i.e. the MSB equals a value of logical
"1", the output value of the AND-gate 404 is also "1". In all other situations, the
output value of the AND-gate 404 is A0". Therefore the most significant bit of the
first and the third register is reset, i.e. set to "0", when they have both become "1".
Hereby, an overflow is avoided in such a manner that the output signal of the phase

20   comparator continuously reflects the phase difference between the two input signals
supplied thereto. Optionally, a similar reset may be implemented for not only MSB,
but for any bit of the digital number.

Fig. 5 illustrates a phase-locked loop including an incremental phase comparator, ie.

25   a phase comparator according to the invention. As shown in Fig. 5 a, the output of
the incremental phase comparator (IPC) 501, i.e. is connected to a voltage
controlled oscillator 503 via a loop filter 502. A reference signal is connected to a
first input of the incremental phase comparator 501, i.e. to the input of the first
register 208 (see Figs. 2, 3 or 4), and the output of the voltage controlled oscillator

30   503 is connected to a second input of the incremental phase comparator 501 via a
frequency divider 504. As illustrated in Figs. 2, 3 and 4, the second input of the
incremental phase comparator 501 may be connected to third register 211. Hereby,
when an oscillation reference signal and an output signal of a voltage controlled
oscillator is supplied as the first and the second input signals to the trigger means

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205, 206, respectively, and when the second and the fourth registers 209, 212 are given a value representing a predefined phase step, the output of the first and the second accumulator represents an accumulated phase value of the reference signal and an accumulated phase value of the output of the voltage controlled oscillator,
5   respectively.

In Fig. 5 b is illustrated how the incremental phase comparator 501 may be composed of a first and a second multiplication block 505, 506 corresponding to blocks 201 and 202, respectively, of Figs. 2, 3 or 4, and means or subtraction
10   means for obtaining a phase error 507 from the outputs of blocks 505 and 506. For block 505 the integer N_R is given as a multiplicand, corresponding to the predetermined phase step value N_R of register 209, and for block 506 N_V is given as a multiplicand, corresponding to the predetermined phase step value N_V of register 212.

15   ^{a}

It has been found by the present inventors that if the systems of the block diagrams of Figs. 3 and 4 are implemented using a standard implementation of the AND-functions and the digital-to-analogue converter (DAC) functions, then it may be difficult to maintain the pulse bandwidth product through the system. A solution to
20   this problem may be to merge the AND and DAC functions together as illustrated in Fig. 6, which shows two blocks 610, 620, where each block has a first one-bit combined logic digital-to-analogue converter (logic DAC) according to the invention. Each logic DAC 610, 620, has switches 611-614, 621-624, a first current line 615, 625, a second current line 616, 626, and a constant current source 617, 627. The
25   circuits 610, 620 are using a logic which may be denoted complementary current mode logic, where both the true and the inverse of an input signal is used to control the switches.

In Fig. 6 two digital signals N_{Rk} and N_{Vk} together with their inverse signals are input
30   to the circuits 610, 620. Here N_{Rk} may represent the value of bit k in a first digital signal N_R and N_{Vk} may represent the value of bit k in a second digital signal N_V, where N_R and N_V both have N bits, with the least significant bit having k=0 and the most significant bit having k= (N-1). According to an embodiment of the invention N_R may be the output of the first accumulator 201 and N_V may be the output of the

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second accumulator 202. For block 610, N_{Rk} is controlling switch 611, the inverse of N_{Rk} is controlling switch 612, the inverse of N_{Vk} is controlling switch 613, and N_{Vk} is controlling switch 614. The switches 611-614, 621-624 may be controlled so that they are closed by a logic "1" and open by a logic "0". From Fig. 6 it is seen for block

5   610 that when N_{Rk} and the inverse of N_{Vk} both represents a logic "1", then the circuit 610 is in a first conductive state, in which the constant current source 617 draws current from the first current line 615. For all other logic combinations of N_{Rk} and the inverse of N_{Vk} then the circuit 610 is in a second conductive state, in which the constant current source 617 draws current from the second current line 616. The

10   current drawn from the first current line 615 of circuit 610 may be denoted $I_{Up}k$, and may represent a current output of the logic-DAC circuit 610. From the above discussion is should be clear that the logic operation performed by circuit 610 is a logic AND of the signals N_{Rk} and the inverse of N_{Vk}, when the current of the first current line 615 is taken as output.

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For block 620, N_{Vk} is controlling switch 621, the inverse of N_{Vk} is controlling switch 622, the inverse of N_{Rk} is controlling switch 623, and N_{Rk} is controlling switch 624. From Fig. 6 it is seen for block 620 that when N_{Vk} and the inverse of N_{Rk} both represents a logic "1", then the circuit 620 is in a first conductive state, in which the

20   constant current source 627 draws current from the first current line 625. For all other logic combinations of N_{Vk} and the inverse of N_{Rk} then the circuit 620 is in a second conductive state, in which the constant current source 627 draws current from the second current line 626. The current drawn from the first current line 625 of circuit 620 may be denoted $I_{Down}k$, and may represent a current output of the logic-

25   DAC circuit 620. From the above discussion is should be clear that the logic operation performed by circuit 620 is a logic AND of the signals N_{Vk} and the inverse of N_{Rk}, when the current of the first current line 625 is taken as output.

A number of circuits 610 corresponding to the number of bits of the signals N_R and

30   N_V may be arranged so that each circuit 610 has input signals corresponding to the same bit number k of N_R and the inverse of N_V, and the corresponding current outputs $I_{Up}k$ may be used to obtain a resulting first analogue output or representation of the bit by bit AND operation of the signals N_R and the inverse of N_V.

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Similarly, a number of circuits 620 corresponding to the number of bits of the signals N_R and N_V may be arranged so that each circuit 620 has input signals corresponding to the same bit number k of N_V and the inverse of N_K, and the corresponding current outputs $I_{Down}k$ may be used to obtain a resulting second analogue output or

5   representation of the bit by bit AND operation of the signals N_V and the inverse of N_R.

For the logic DAC circuits of Fig. 6 other logic operations such as NAND, OR or NOR can be obtained by having the signals N_{Rk}, the inverse of N_{Rk}, N_{Vk} and the

10   inverse of N_{Vk} controlling the switches 611-614, 621-624 accordingly.

It should also be noted that for circuit 610 the same output is obtained if switch 611 is controlled by the inverse of N_{Vk}, N_{Vk} is controlling switch 612, N_{Rk} is controlling switch 613, and the inverse of N_{Rk} is controlling switch 614. In the same way, for

15   circuit 620 the same output is obtained if switch 621 is controlled by the inverse of N_{Rk}, N_{Rk} is controlling switch 622, N_{Vk} is controlling switch 623, and the inverse of N_{Vk} is controlling switch 624.

According to the present invention, there is also provided a combined logic digital-to-

20   analogue (combined logic DAC), which may perform the functions of blocks 610 and 620 by using a single constant current source. By using a single constant current source, the max. values of $I_{Up}k$ and $I_{Down}k$ may be substantially equal. This is illustrated in Fig. 7, which shows a combined logic digital-to-analogue converter 710 according to the invention performing the same function as the two blocks 610 and

25   620 of Fig. 6. The combined logic DAC 710 has switches 711-713, 721-723, a first current line 715, a second current line 716, a third current line 725, a fourth current line 726, and a constant current source 717. It is preferred that the second and fourth current lines 716, 726 are supplied from the same current line, as illustrated in Fig. 7.

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In Fig. 7 the two digital signals N_{Rk} and N_{Vk} together with their inverse signals are input to the circuit 710 where the inverse of N_{Vk} is controlling switch 711, N_{Vk} is controlling switch 712, N_{Rk} is controlling switch 713, N_{Vk} is controlling switch 721, the inverse of N_{Vk} is controlling switch 722, and the inverse of N_{Rk} is controlling switch

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723. Also here, the switches 711-713, 721-724 may be controlled so that they are closed by a logic "1" and open by a logic "0". From Fig. 7 it is seen that when N_{Rk} and the inverse of N_{Vk} both represents a logic "1", then the circuit 710 is in a first conductive state, in which the constant current source 717 draws current from the

5   first current line 715. It is further seen that when N_{Vk} and the inverse of N_{Rk} both represents a logic "1", then the circuit 710 is in a third conductive state, in which the constant current source 717 draws current from the third current line 725.

For all other logic combinations of N_{Rk} and N_{Vk} then the circuit 710 is in a second

10   conductive state, in which the constant current source 717 draws current from the second current line 716 or the fourth current line 726, where the second and the fourth current lines 716, 726 may be supplied from the same supply line. The current drawn from the first current line 715 may be denoted $I_{Up}k$, and may correspond to the current output of the logic-DAC circuit 610, and the current drawn from the third

15   current line 725 may be denoted $I_{Down}k$, and may correspond to the current output of the logic-DAC circuit 620.

From the above discussion is should be clear that the logic operation performed by circuit 710 is a logic AND of the signals N_{Rk} and the inverse of N_{Vk}, when the current

20   of the first current line 715 is taken as output, and a logic AND of the signals N_{Vk} and the inverse of N_{Rk}, when the current of the third current line 725 is taken as output.

Also here, a number of circuits 710 corresponding to the number of bits of the signals N_R and N_V may be arranged so that each circuit 710 has input signals

25   corresponding to the same bit number k of N_R and N_V and their inverese, and the corresponding current outputs $I_{Up}k$ may be used to obtain a resulting first analogue output or representation of the bit by bit AND operation of the signals N_R and the inverse of N_V, while the corresponding current outputs $I_{Down}k$ may be used to obtain a resulting second analogue output or representation of the bit by bit AND operation

30   of the signals N_V and the inverse of N_R.

Again, for the combined logic DAC circuit of Fig. 7 other logic operations such as NAND, OR or NOR can be obtained by having the signals N_{Rk}, the inverse of N_{Rk},

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N_{Vk} and the inverse of N_{Vk} arranged for controlling the switches 711-713, 721-723 accordingly.

In Fig. 8 is shown a circuit example of a combined logic digital-to-analogue
5   converter 810 according to Fig. 7. For the logic DAC 810 the components have the
same numbering as for the circuit 710 except that the first digit is 8 instead of 7. The
circuit 810 is implemented in NMOS technology using NMOS transistors for the
switches 811-813, 821-823. However, a circuit having the same logic functionality
may be produced in PMOS technology using PMOS transistors for the switches
10   811-813, 821-823. It should be noted that the circuits 610, 620 may also be
produced using NMOS technology with NMOS transistors for the switches or PMOS
technology with PMOS transistors for the switches.

Fig. 9 shows another circuit example for a combined logic digital-to-analogue
15   converter 910 according to Fig. 7. For the logic DAC 910 the components have the
same numbering as for the circuit 910 except that the first digit is 9 instead of 7. The
circuit 910 is also implemented using NMOS technology, and compared to the circuit
810, the circuit 910 has a first cascode stage 930 inserted in the first current line 915
and a second cascode stage 931 inserted in the third current line 925. The NMOS
20   transistors of the stages 930, 931 are controlled by a reference gate voltage Vbias.
The use of the cascode stages 930, 931 may in some cases lead to an improved
performance.

A combination of the two one-bit logic DAC's 610 and 620 of Fig. 6 may be
25   considered as a combined one-bit logic DAC, hereby referring to the inputs being
the two single bits N_{Rk} and N_{Vk} together with their inverse signals. The combined
one-bit logic DAC is using the two constant current sources 617, 627 and has the
two current outputs $I_{Up}k$ and $I_{Down}k$. In the same way the combined logic DAC 710
may also be considered as a combined one-bit logic DAC, having the same input
30   signals and current outputs as for the combination of 610 and 620, but only using a
single constant current source.

By combining a number of such one-bit logic DAC circuits, several different multi-bit
logic DAC's may be implemented. One such basic implementation uses a resistor

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network, which may be the well-known R2R network. This is illustrated in Fig. 10, which shows a circuit 1010 comprising four one-bit combined logic DAC's according to the embodiment shown in Fig. 7, and having a R2R resistor network. The circuit 1010 may thus be considered as a 4-bit combined logic DAC, having the four one-bit
5   combined logic DAC's 1011, 1012, 1013, 1014 and a resistor-to-resistor, R2R, network arranged as shown on Fig. 10. Here, each of the one-bit logic DAC's 1011-1014 has two current outputs $I_{Up}k$ and $I_{Down}k$, respectively and inputs N_{Rk}, N_{Vk}, together with their inverse signals, where k has the values 0,1, 2, and 3. Each one-bit logic DAC 1011-1014 has a single constant current source with the same current
10   value, where the current I is set equal to a value I_{MSB}. A voltage drop is generated in the R2R network by the currents $I_{Up}k$ resulting in a first analogue voltage output V_{Up}, and a voltage drop is generated in the R2R network by the currents $I_{Down}k$ resulting in a second analogue voltage output V_{Down}.

15   The functions of the combined one-bit logic DAC's 1011-1014 of the circuit 1010 may also be performed by using combined one-bit logic DAC's each comprising the circuits 610 and 620. In this case, each of the circuits 1011-1014 would then have two constant current sources of the same value, which would then be 1/2 I_{MSB}.

20   Another implementation of a multi-bit logic DAC is illustrated in Fig. 11, which shows another circuit example of a 4-bit logic DAC, which may be denoted a binary exponential current logic DAC. Here a circuit 1110 comprises four one-bit combined logic DAC's 1111-1114. Here, each of the one-bit logic DAC's 1111-1114 has two current outputs $I_{Up}k$ and $I_{Down}k$, respectively and inputs N_{Rk}, N_{Vk}, together with their
25   inverse signals, where k has the values 0,1, 2, and 3. According to one embodiment of the invention each of the circuits 1111-1114 may be a combined one-bit logic DAC according to the circuit 710 of Fig. 7. For binary exponential current logic DAC's the current drawn by the constant current sources will not be equal, so for circuit 1111, corresponding to k=0, the current of the constant current source is set
30   to $I=I_{LSB}2^0$, for circuit 1112 having k=1, the current is set to $I=I_{LSB}2^1$, for circuit 1113 having k=2, the current is set to $I=I_{LSB}2^2$, and for circuit 1114 having k=3, the current is set to $I=I_{LSB}2^3$. Thus, for a N-bit binary exponential current logic DAC, the value of the constant current source corresponding to the one-bit logic DAC of bit k is set to $I=I_{LSB}2^k$, where k varies from 0 to N-1.

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The functions of the combined one-bit logic DAC's 1111-1114 of the circuit 1110 may also be performed by using combined one-bit logic DAC's each comprising the circuits 610 and 620. In this case, each of the circuits 1111-1114 would then have

5   two constant current sources of the same value, which would then be 1/2 $I_{LSB}2^k$.

For the circuit 1110 of Fig. 11, each of the current outpus $I_{Up}k$ of the circuits 1111-1114 is drawing current from the same supply line 1115 resulting in a first analogue current output I_{Up}, and each of the current outpus $I_{Down}k$ of the circuits 1111-1114 is

10   drawing current from the same supply line 1116 resulting in a second analogue current output I_{Down}.

For the circuit 1110 It should be understood that it may be difficult to implement a number of current sources having different values varying with the bit number k as

15   I= $I_{LSB}2^k$. Thus, according to the present invéntion there is provided another solution, for a multi-bit binary exponential current logic DAC. Instead of using a constant current source drawing a larger current, there is used a number of combined one-bit logic DAC's, which are arranged in parallel having the same inputs and having the current outputs $I_{Up}k$ and $I_{Down}k$ drawing current from the same supply line and having

20   constant current sources of equal current I = I_{LSB}. Here, the number of parallel combined one-bit logic DAC's corresponding to bit k should be chosen so that the current of the parallel constant current sources equal the current I= $I_{LSB}2^k$, resulting in 2^k parallel one-bit logic DAC's for bit k, where k varies from 0 to N-1. So, for the 4-bit logic DAC 1110 of Fig. 11, then for circuit 1111, corresponding to k=0, the

25   number of combined one-bit logic DAC's is 1, for circuit 1112 having k=1, the number of parallel combined one-bit logic DAC's is 2, for circuit 1113 having k=2, the number of parallel combined one-bit logic DAC's is 2^2 = 4, and for circuit 1114 having k=3, the number of parallel combined one-bit logic DAC's is 2^3 = 8.

30   The parallel combined one-bit logic DAC's used for the multi-bit binary exponential current logic DAC may correspond to the circuit 710 of Fig. 7, or they may correspond to the combined one-bit logic DAC's comprising the circuits 610 and 620. In this latter case, each of the parallel combined one-bit logic DAC's would then have two constant current sources of the same value, which would then be 1/2 I_{LSB}.

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Another multi-bit logic DAC according to the present invention may be implemented
by use of a capacitor network, which may be a C2C (capacitor to capacitor) network
arranged similar to the R2R network illustrated in Fig. 10. The present invention also
5   covers embodiments of multi-bit logic DAC's comprising both a multi-bit logic DAC
using a R2R network and a multi-bit logic DAC using a C2C network. This is
illustrated in Fig. 12, in which a circuit 1210 is shown being combination of the 4-bit
logic DAC of Fig. 10, 1211, using a resistor network, R2R, and a 4-bit logic DAC,
1212, using a capacitor network, C2C. The circuit 1210 further comprises a first
10   adder circuit 1213 for adding voltage outputs $V_{Up}R$ and $V_{Up}C$ from 1211 and 1212,
respectively, and a second adder circuit 1214 for adding voltage outputs $V_{Down}R$ and
$V_{Down}C$ from 1211 and 1212, respectively, to thereby generate corresponding first
and second analogue voltage outputs.

15   A multi-bit logic DAC according to the invention may be used in an incremental
phase comparator according to the invention. This phase comparator may again be
used in a phase-locked loop (PLL) structure. Here, the loop filter function of the PLL
structure can be applied on the output of the multi-bit logic DAC, either as a passive
or active filter depending on which multi-bit logic DAC structure is used and the
20   requirements of the system. By applying the filter function, a subtraction of the
second analogue output from the first analogue output may be part of the filter
function.

Fig. 13 shows an example of an active loop filter 1311 using the circuit 1010 of Fig.
25   10. The filter 1311 comprises an OP-AMP being arranged as an integrator to
implement a secord order PLL. The first input of the OP-AMP is the V_{Up} output of
circuit 1010, and the second input is the V_{Down}, output. By using V_{Up} and V_{Down} as the
inputs for the OP-AMP, V_{Down} is subtracted from V_{Up}.

30   Fig. 14 shows an example of a current mode transcondutance integrator
implementing a first order filter of a second order PLL 1411 using the circuit 1110 of
Fig. 11. The filter 1411 comprises a capacitor C connected in series with a resistor
R, with the resistor R further being connected to the first analogue output I_{Up} of
circuit 1110 and the capacitor C further being connected to the second analogue

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output I_{Down} of circuit 1110. First and second constant current sources 1412, 1413 are supplying current to the first and second analogue current outputs I_{Up} and I_{Down}. The resulting filter function is the difference between the I_{Up} signal and I_{Down} signal.

5   When comparing the phase-locked loop according to the invention with the prior art phase-locked loop of Fig. 1, it is found that the incremental phase comparator (IPC) replaces a phase detector according to the prior art, i.e. it has the same function as the prior art phase-locked loop of figure 1, but has a much better bandwidth and consequently faster lock-in time.

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The invention has been described with a preferred embodiment. It is, however, possible to make changes and alterations to the shown example, while staying within the inventions idea. As an example, it is in the above description hinted that the digital numbers in the registers always are the same or will only change

15   occasionally. It is, however, as an example possible to continuously change the digital numbers in the registers and thereby produce a pulse wide modulation of the output signal with the result that different phase and frequency modulation schemes (QPSK, FSK, GFSK, etc.) are achieved.

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CLAIMS

1.   A phase-locked loop comprising:
      a voltage controlled oscillator for generating an output signal and having a
frequency control input for controlling the frequency of the output signal, and
      a phase comparator for deriving a control signal from a phase error detected
in response to the received output signal and a reference signal, said control signal
being coupled to the frequency control input of said voltage controlled oscillator,
wherein the phase comparator includes:
      a first accumulator adapted to add a first predefined phase step value to a first
accumulated phase value in response to a reoccurring event in the reference signal,
      a second accumulator adapted to add a second predefined phase step value
to a second accumulated phase value in response to a reoccurring event in the
received output signal, and
      means or arithmetic means for determining the phase error from the obtained
first and second accumulated phase values.

2.   A phase-locked loop according to claim 1, further comprising a divider for
dividing the frequency of the output signal, whereby the received output signal
received by the phase comparator is a frequency-divided output signal.

3.   A phase-locked loop according to claim 1 or 2, wherein the arithmetic means
are subtracting means for determining the phase error by a subtraction between the
obtained first and second accumulated phase values.

4.   A phase-locked loop according to claim 3, wherein the subtracting means are
adapted for subtracting the second accumulated phase value from the first
accumulated phase value.

5.   A phase-locked loop according to any one of the claims 1-4, wherein the
phase comparator includes a digital-to-analogue converter adapted to convert the
phase error and thereby to generate an analogue output signal.

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6.   A phase-locked loop according to any one of the claims 1-4, wherein the phase comparator includes a converter circuit having:

means for performing a first logic bit by bit AND operation of the output of the first accumulator and the inverted output of the second accumulator, and for

5   generating a first analogue representation of said first logic bit by bit AND operation, and

means for performing a second logic bit by bit AND operation of the output of the second accumulator and the inverted output of the first accumulator, and for generating a second analogue representation of said second logic bit by bit AND

10   operation.

7.   A phase-locked loop according to claim 6, wherein the converter circuit comprises current mode logic circuits giving a current output for a two input AND operation, said current output being used for generating an analogue representation

15   for a bit by bit AND operation.

8.   A phase-locked loop according to claim 6 or 7, wherein the arithmetic means are adapted to obtain one or more analogue phase error signals based on the second analogue representation of the second logic bit by bit AND operation and the

20   first analogue representation of the first logic bit by bit AND operation.

9.   A phase-locked loop according to claim 8, wherein the arithmetic means comprises subtraction means being adapted for performing an analogue subtraction of the second analogue representation from the first analogue representation.

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10.   A phase-locked loop according to any one of the claims 1-5, wherein the phase comparator includes a first and a second digital-to-analogue converter adapted to convert the first and the second accumulated phase value and thereby to generate analogue representations thereof, and that the arithmetic means are

30   adapted to perform an analogue subtraction of the analogue representation of the second accumulated phase value from the analogue representation of the first accumulated phase value.

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11.   A phase-locked loop according to claim 10, wherein the phase comparator includes a first and a second AND-means, where the output of said first AND-means is connected to the first digital-to-analogue converter, whereby the first accumulator is connected to a first non-inverting input of said first AND-means and whereby the

5   second accumulator is connected to a first inverting input of said first AND-means, the output of said second AND-means being connected to said second digital-to-analogue converter, and that said second accumulator further is connected to a first non-inverting input of said second AND-means, said first accumulator further being connected to a first inverting input of said second AND-means.

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12.   A phase-locked loop according to any one of the claims 1-11, wherein the phase comparator includes a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator, and a third AND-means, where the output of said third AND-means is

15   connected to said first and said second reset means of said first and said second accumulator, where the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means.

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13.   A method for determining a phase error in response to a first signal and a second signal, said method comprising the steps of:

        generating a first reoccurring trigger event in response to the first signal,

        generating a second reoccurring trigger event in response to the second

25   signal,

        incrementing a first phase value by a first predetermined increment value when the first trigger event occurs to obtain a first accumulated phase value,

        incrementing a second phase value by a second predetermined increment value when the second trigger event occurs to obtain a second accumulated phase

30   value, and

        calculating or determining said phase error based on obtained first and second accumulated phase values.

14. A method according to claim 13, said method comprising the step of frequency dividing the first signal and/or the second signal, whereby the generation of the first and/or second reoccurring trigger event is performed in response to the frequency divided first and/or second signal, respectively.

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15. A method according to claim 13 and 14, wherein the calculation of the phase error is based on a subtraction of said second accumulated phase value from said first accumulated phase value.

10   16. A method according to any one of the claims 13-15, wherein the first accumulated phase value, the second accumulated phase value and the phase error are represented by binary numbers.

17. A method according to any one of the claims 13-15, wherein the first

15   accumulated phase value and the second accumulated phase value are represented by binary numbers and the phase error is represented by an analogue signal.

18. A method according to claim 17, said method further comprising the steps of:

20   performing a first logic bit by bit AND operation of the first accumulated phase value and the inverted second accumulated phase value, and generating a first analogue representation of said first logic bit by bit AND operation, and performing a second logic bit by bit AND operation of the second accumulated phase value and the inverted first accumulated phase value, and generating a

25   second analogue representation of said second logic bit by bit AND operation.

19. A method according to claim 18, wherein the calculation of the phase error comprises generating one or more analogue phase error signal based on the second analogue representation of the second logic bit by bit AND operation and the

30   first analogue representation of the first logic bit by bit AND operation.

20. A method according to claim 19, wherein the calculation of the phase error comprises performing an analogue subtraction of the second analogue representation from the first analogue representation.

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21.   A method according to any one of the claims 16-20, wherein the most significant bit of the first accumulated phase value and the most significant bit of the second accumulated phase value are reset when the most significant bit of both said first accumulated phase value and said second accumulated phase value are simultaneously 1.

22.   A method according to claim 21, wherein two equal bits are reset whenever these bits are 1 at the same time.

23.   A phase comparator for carrying out the method in accordance to claim 13-22, wherein the first signal is a reference signal and the second signal is an input signal, said phase comparator including:

a first accumulator adapted to add a first predefined phase step value to a first accumulated phase value in response to a reoccurring event in said reference signal,

a second accumulator adapted to add a second predefined phase step value to a second accumulated phase value in response to a reoccurring event in said input signal, and

means or arithmetic means for determining the phase error based on the second accumulated phase value and the first accumulated phase value.

24.   A phase comparator according to claim 23, wherein the arithmetic means comprises subtracting means for determining the phase error by subtracting the second accumulated phase value from the first accumulated phase value.

25.   A phase comparator according to claim 23 or 24, wherein the phase comparator includes a digital-to-analogue converter adapted to convert the phase error and thereby to generate an analogue output signal.

26.   A phase comparator according to any one of the claims 23-25, wherein the phase comparator includes a converter circuit having:

means for performing a first logic bit by bit AND operation of the output of the first accumulator and the inverted output of the second accumulator, and for

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generating a first analogue representation of said first logic bit by bit AND operation, and

means for performing a second logic bit by bit AND operation of the output of the second accumulator and the inverted output of the first accumulator, and for

5   generating a second analogue representation of said second logic bit by bit AND operation.

27.   A phase comparator according to claim 26, wherein the converter circuit comprises current mode logic circuits giving a current output for a two bit AND

10   operation, said current output being used for generating an analogue representation for a bit by bit AND operation.

28.   A phase comparator according to claim 26 or 27, wherein the arithmetic means are adapted to obtain one or more analogue phase error signals based on

15   the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

29.   A phase comparator according to claim 28, wherein the arithmetic means comprises subtraction means being adapted for performing an analogue subtraction

20   of the second analogue representation from the first analogue representation.

30.   A phase comparator according to claim 23 or 24, wherein the phase comparator includes a first and a second digital-to-analogue converter adapted to convert the first and the second accumulated phase value and thereby to generate

25   analogue representations thereof, and that the subtracting means are adapted to perform an analogue subtraction of the analogue representation of said second accumulated phase value from the analogue representation of said first accumulated phase value.

30   31.   A phase comparator according to claim 30, wherein the phase comparator includes a first and a second AND-means, where the output of said first AND-means is connected to a first digital-to-analogue converter, whereby a first accumulator is connected to a first non-inverting input of said first AND-means, and whereby a second accumu-lator is connected to a first inverting input of said first AND-means,

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the output of said second AND-means being connected to said second digital-to-analogue converter, and that said second accumulator further is connected to a first non-inverting input of said second AND-means, said first accumulator further being connected to a first inverting input of said second AND-means.

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32.   A phase comparator according to any one of the claims 23-31, wherein the phase comparator includes a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator and a third AND-means, where the output of said third AND-means is
10   connected to said first and said second reset means of said first and said second accumulator, where the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means.

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33.   A converter circuit for obtaining an analogue presentation of a digital input signal or of a logical operation on several digital input signals, at least one of the digital input signals having at least 2 bits, said circuit comprising
        a number of current mode logic circuits, CML circuits arranged in modules,
20   with each CML circuit having one or more logic input signals, a first current line, a second current line and a constant current source, each of said CML circuits further comprising means for switching the constant current source between a first conductive state, in which the current source draws or delivers current via the first current line, and a second conductive state, in which the current source draws or
25   delivers current via the second current line, said switching being controlled by at least one of the logic input signals, wherein
        a first module has at least one CML circuit, with each CML circuit of the first module having a first logic input signal representing the first bit value of a first digital input signal and providing a first control signal for the switching between the first and
30   the second conductive state, and
        a second module has at least one CML circuit, with each CML circuit of the second module having a first logic input signal representing the second bit value of the first digital input signal and providing a first control signal for the switching between the first and the second conductive state.

34.   A converter circuit according to claim 33, wherein the first digital signal has N-bits, and wherein for each bit k, where k is selected as an integer larger than or equal to zero and smaller than or equal to N-1, there is a corresponding module k having at least one CML circuit, with each CML circuit of the module k having a first logic input signal representing the value of the corresponding bit k of the first digital input signal and providing a first control signal for the switching between the first and the second conductive state.

35.   A converter circuit according to claim 33 or 34, wherein the current drawn from or delivered to said first current lines of the CML circuits arranged in the modules is used for generating a first analogue output for the converter circuit.

36.   A converter circuit according to any one of the claims 33-35, wherein at least part or all of the CML circuits have said logic input signals together with the inverse of said logic input signals as input signals for controlling the switching between the first and the second conductive state.

37.   A converter according to any one of the claims 34-36, wherein for each module k, there is one corresponding CML circuit.

38.   A converter circuit according to claims 35 and 37, wherein the current drawn from or supplied to the first lines of the CML circuits of the modules is used for generating the first analogue output as a voltage output via a first resistor network or via a first capacitor network.

39.   A converter according to any one of the claims 34-36, wherein for each module k, there are 2^k corresponding CML circuits.

40.   A converter circuit according to claims 35 and 37, wherein the sum of the current drawn from or supplied to the first lines of the CML circuits of the modules is used for generating the first analogue output as a current output.

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41.   A converter circuit according to any one of the claims 33-40, wherein for the first module, the logic of each CML circuit is designed so that in order for the first logic input signal to control the state of a CML circuit to be in the first conductive state, the first bit of the first digital signal shall be active.

42.   A converter circuit according to any one of the claims 33-41, wherein for the second module, the logic of each CML circuit is designed so that in order for the first logic input signal to control the state of a CML circuit to be in the first conductive state, the second bit of the first digital signal shall be active.

43.   A converter circuit according to any one of the claims 34-42, wherein for module k, the logic of each CML circuit is designed so that in order for the first logic input signal to control the state of a CML circuit to be in the first conductive state, the corresponding bit k of the first digital signal shall be active.

44.   A converter circuit according to any one of the claims 33-43, wherein a part or all of the CML circuits of said modules are designed as buffer or inverter circuits having only one logic input signal together with the inverse of said logic signal, said logic signal representing a corresponding bit of the first digital signal.

45.   A converter circuit according to any one of the claims 33-43, said converter circuit being designed for obtaining an analogue presentation of a bit by bit logic operation of the first digital signal and a second digital signal, said first and second digital signals having the same number of bits, wherein the CML circuits having a first logic input signal representing the value of a corresponding bit of the first digital signal are designed as first logic operating circuits, each said first logic operating circuit further having as input signal a second logic input signal representing a value of a corresponding bit of the second digital signal, and said second logic input signal providing a second control signal for the switching between the first and the second conductive state.

46.   A converter circuit according to claim 45, wherein each first logic operating circuit is designed for performing a logic operation selected between the following logic operations: AND, NAND, OR, NOR, XOR or XNOR.

47. A converter circuit according to claim 45 or 46, wherein said first logic operating CML circuits also have as input signals the inverse signals of the first and second logic input signals.

48. A converter circuit according to any one of the claims 45-47, wherein the logic of said first logic operating circuits is designed as first AND operating circuits, said AND operating circuits being designed so that in order for the first and second logic input signals to control the state of a CML circuit to be in the first conductive state, the corresponding bit values of the first digital signal and the second digital signal shall both be active.

49. A converter circuit according to claim 48, wherein said switching means of a first AND operating CML circuit comprises a first switch being controlled by the first logic signal, a second switch being controlled by the inverse of the first logic signal, a third switch being controlled by the second logic signal, and a fourth switch being controlled by the inverse of the second logic signal.

50. A converter circuit according to claim 49, wherein said switches are arranged so that the CML circuit is in the first conductive state drawing or delivering current via the first current line through the first and third switches when the bit values corresponding to the first and second logic signals are both active, and
so that the CML circuit is in the second conductive state drawing or delivering current via the second current line through the second and the third switches when the bit value corresponding to the first logic signal is non-active and the bit value corresponding to the second logic signal is active, or through the fourth switch when the bit values corresponding to the first and second logic signals are both non-active.

51. A converter circuit according to any one of the claims 45-50, wherein the first and second logic signals being input to the same first logic operating CML circuit correspond to the same bit number of the first and the second digital signal, respectively.

52.   A converter circuit according to any one of the claims 45-51, said converter circuit further being designed for obtaining an analogue presentation of a bit by bit logic operation on a third and a fourth digital signal, said third and fourth digital signals having the same number of bits and having at least 2 bits.

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53.   A converter circuit according to claim 52, wherein the first, second, third and fourth digital signals have the same number of bits.

54.   A converter circuit according to claims 52 or 53, said converter circuit further

10   comprising a number of CML circuits being designed as second logic operating circuits, with each second logic operating circuit having at least a first logic input signal representing the value of a corresponding bit of the third digital signal and a second logic input signal representing the value of a corresponding bit of the fourth digital signal, a third current line, a fourth current line and a constant current source,

15   each of said second logic operating circuits further comprising means for switching the constant current source between a first conductive state, in which the current source draws or delivers current via the third current line, and a second conductive state, in which the current source draws or delivers current via the fourth current line, said switching being controlled by at least said first and second logic input

20   signals.

55.   A converter circuit according to claim 54, wherein the current drawn from or delivered to the first current lines of the first logic operating circuits arranged in the modules is used for generating a first analogue output for the converter circuit, and

25   wherein the current drawn from or delivered to the third current lines of the second logic operating circuits arranged in the modules is used for generating a second analogue output for the converter circuit.

56.   A converter circuit according to claim 54 or 55, wherein each second logic

30   operating circuit is designed as a logic operating circuit selected between the following logic operating circuits: AND, NAND, OR, NOR, XOR or XNOR logic operating circuit.

57.   A converter circuit according to any one of the claims 54-56, wherein the first and the second logic operating circuits are both designed for performing the same logic operation.

5   58.   A converter circuit according to any one of the claims 54-57, wherein said second logic operating CML circuits also have as input signals the inverse signals of the first and second logic input signals.

59.   A converter circuit according to any one of the claims 54-58, wherein the
10   second logic operating circuits are designed as second AND operating circuits, to thereby obtain an analogue presentation of a bit by bit AND operation on the third and the fourth digital signals.

60.   A converter circuit according to claim 59, wherein the third and fourth digital
15   signals have P-bits, and wherein for each bit m, where m is selected as an integer larger than or equal to zero and smaller than or equal to P-1, there is a corresponding module m having at least one second AND operating circuit, with each second AND operating circuit of the module m having a first logic input signal representing the value of the corresponding bit m of the third digital signal and
20   providing a first control signal for the switching between the first and the second conductive state, and with each second AND operating circuit of the module m having a second logic input signal representing the value of the corresponding bit m of the fourth digital signal and providing a second control signal for the switching between the first and the second conductive state.

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61.   A converter circuit according to claim 59 or 60, wherein the logic of said CML circuits being designed as second AND operating circuits is designed so that in order for the first and second logic input signals to control the state of a second AND operating circuit to be in the first conductive state, the corresponding bit values of
30   the third digital signal and the fourth digital signal shall both be active.

62.   A converter circuit according to any one of the claims 59-61, wherein said switching means of a second AND operating circuit comprises a first switch being controlled by the first logic signal, a second switch being controlled by the inverse of

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the first logic signal, a third switch being controlled by the second logic signal, and a fourth switch being controlled by the inverse of the second logic signal.

63.   A converter circuit according to claim 62, wherein said switches are arranged so that the second AND operating circuit is in the first conductive state drawing or delivering current via the third current line through the first and third switches when the bit values corresponding to the first and second logic input signals are both active, and

so that the second AND operating circuit is in the second conductive state drawing or delivering current via the fourth current line through the second and the third switches when the bit value corresponding to the first logic signal is non-active and the bit value corresponding to the second logic signal is active, or through the fourth switch when the bit values corresponding to the first and second logic input signals are both non-active.

64.   A converter circuit according to any one of the claims 54-63, wherein the first and second logic signals being input to the same second logic operating circuit correspond to the same bit number of the third and the fourth digital signals, respectively.

65.   A converter circuit according to any one of the claims 52-64, wherein said third and fourth digital signals are the inverse signals of the first and second digital signals, respectively, or the inverse signals of the second or first digital signals, respectively.

66.   A converter according to claim 37 and any one of the claims 60-65, wherein for each module m, there is one corresponding second logic operating circuit.

67.   A converter according to claim 39 and any one of the claims 60-65, wherein for each module m, there are 2^m corresponding second AND operating circuits.

68.   A converter circuit according to any one of the claims 33-43, said converter circuit being designed for obtaining an analogue presentation of a bit by bit first logic operation on the first digital signal and a second digital signal, and for obtaining an

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analogue presentation of a bit by bit first logic operation of the inverse signals of the first and second digital signals, said first and second digital signals having the same number of bits.

5   69.   A converter circuit according to claim 68, wherein the CML circuits having a first logic input signal representing the value of a corresponding bit of the first digital signal are designed as combined logic operating circuits, each combined logic operating circuit further having:

       a second logic input signal representing a value of a corresponding bit of the
10   second digital signal, and a third current line;

       said switching means further being adapted for switching the constant current source between the first conductive state, in which the current source draws or delivers current via the first current line, the second conductive state, in which the current source draws or delivers current via the second current line, and a third
15   conductive state in which the current source draws or delivers current via the third current line; and

       said first and second logic input signals providing corresponding first and second control signals for the switching between the first, second and third conductive states.

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       70.   A converter circuit for obtaining an analogue presentation of a bit by bit first logic operation on a first digital signal and a second digital signal, and for obtaining an analogue presentation of a bit by bit first logic operation of the inverse signals of the first and second digital signals, said first and second digital signals having the
25   same number of bits, said circuit comprising:

       a number of current mode logic circuits, CML circuits, being designed as combined logic operating circuits, with each combined logic operating circuit having a first logic input signal representing the value of a corresponding bit of the first digital signal and a second logic input signal representing a value of a corresponding
30   bit of the second digital signal, a first current line, a second current line, a third current line and a constant current source, each of said combined logic operating circuits further having means for switching the constant current source between a first conductive state, in which the current source draws or delivers current via the first current line, a second conductive state, in which the current source draws or

delivers current via the second current line, and a third conductive state in which the current source draws or delivers current via the third current line; and

said first and second logic input signals providing corresponding first and second control signals for the switching between the first, second and third

5   conductive states.

71.   A converter circuit according to claim 69 or 70, wherein the current drawn from or delivered to the first current lines of the combined logic operating circuits arranged in the modules is used for generating a first analogue output for the

10   converter circuit, and wherein the current drawn from or delivered to the third current lines of the combined logic operating circuits arranged in the modules is used for generating a second analogue output for the converter circuit.

72.   A converter circuit according to any one of the claims 68-71, wherein the

15   converter circuit is designed so that the first logic operation is selected between the following logic operations: AND, NAND, OR, NOR, XOR or XNOR logic operating circuit.

73.   A converter circuit according to any one of the claims 69-72, wherein each

20   combined logic operating circuit is designed as a combined AND operating circuit, to thereby obtain an analogue presentation of a bit by bit AND operation on the first digital signal and the second digital signal, and for obtaining an analogue presentation of a bit by bit AND operation of the inverse signals of the first and second digital signals.

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74.   A converter circuit according to any one of the claims 69-73, wherein each combined logic operating circuit further has a third logic input signal representing the inverse value of the bit corresponding to the first digital signal, and a fourth logic input signal representing the inverse value of the bit corresponding to the second

30   digital signal, said third and fourth logic input signals providing corresponding third and fourth control signals for the switching between the first, second and third conductive states.

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75.   A converter circuit according to claim 73 or 74, wherein the logic of the combined AND operating CML circuits is designed so that in order for the logic input signals to control the state of a combined AND operating circuit to be in:

      the first conductive state, the corresponding bit values of the first digital signal and the second digital signal shall both be active;

      the third conductive state, the corresponding bit values of the first digital signal and the second digital signal shall both be non-active; and

      the second conductive state, the corresponding bit value of the first digital signal shall be non-active with the corresponding bit value of the second digital signal being active, or the corresponding bit value of the first digital signal shall be active with the corresponding bit value of the second digital signal being non-active.

76.   A converter circuit according to any one of the claims 68-75, wherein the first and second logic input signals corresponds to the same bit number of the first and second digital signals, respectively.

77.   A converter circuit according to any one of the claims 73-76, wherein the switching means of the combined AND operating circuit comprises a first switch being controlled by the first logic signal, a second switch being controlled by the third logic signal or the inverse of the first logic signal, a third switch being controlled by the second logic signal, a fourth switch being controlled by the fourth logic signal or the inverse of the second logic signal, a fifth switch being controlled by the third logic signal of the inverse of the first logic signal, and a sixth switch being controlled by the first logic signal.

78.   A converter circuit according to claim 77, wherein said switches are arranged so that the combined AND operating circuit is in:

      the first conductive state drawing or delivering current via the first current line through the first and third switches when the bit values corresponding to the first and second logic signals are both active;

      the third conductive state drawing or delivering current via the third current line through the fifth and fourth switches when the bit values corresponding to the first and second logic signals are both non-active;

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the second conductive state drawing or delivering current via the second current line through the third and second switches when the bit value corresponding to the first logic signal is non-active and the bit value corresponding to the second logic signal is active; and

5   the second conductive state drawing or delivering current via the second current line through the sixth and fourth switches when the bit value corresponding to the first logic signal is active and the bit value corresponding to the second logic signal is non-active.

10   79.   A digital to analogue converter circuit according to any one of the claims 33-78, wherein the number of CML circuits are powered by the same power supply having a positive supply terminal and a negative or ground terminal.

80.   A converter circuit according to any one of the claims 33-79, wherein the
15   constant current sources of each of the CML circuits of said modules or each of the CML circuits are designed to draw or deliver substantially the same current.

81.   A converter circuit according to any one of the claims 39-80, wherein the converter circuit has modules with CML circuits, and wherein for each module
20   corresponding to bit k there are 2^k corresponding CML circuits having a first current line and a second current line, each said first current line being supplied from the same, first supply line.

82.   A converter circuit according to claims 81, wherein the current drawn from or
25   delivered to said first supply line by the first current lines represent a first analogue output signal for the converter circuit.

83.   A converter circuit according to any one of the claims 69-80, wherein the converter circuit has modules with combined logic operating CML circuits, and
30   wherein for each module corresponding to bit k there are 2^k corresponding combined logic operating circuits having a first current line, a second current line and a third current line, each said first current line being supplied from the same, first supply line, and each said third current line being supplied from the same, third supply line.

84.   A converter circuit according to claims 83, wherein the current drawn from or delivered to said first supply line by the first current lines represent a first analogue output signal for the converter circuit, and the current drawn from or delivered to said third supply line by the third current lines represent a second analogue output signal for the converter circuit.

85.   A converter circuit according to any one of the claims 54-82, wherein the converter circuit has modules with second logic operating CML circuits, and wherein for each module corresponding to bit m there are 2^m corresponding CML circuits having a third current line and a fourth current line, each said third current line being supplied from the same, third supply line.

86.   A converter circuit according to claims 85, wherein the current drawn from or delivered to said third supply line by the third current lines represent a second analogue output signal for the converter circuit.

87.   A converter circuit according to claim 37 and any one of the claims 41-80, wherein the converter circuit has modules with CML circuits, and wherein for each module corresponding to bit k there is one corresponding CML circuit having a first current line and a second current line, each said first current line being supplied from the same power supply via a first resistor network or via a first capacitor network having a first voltage output representing a first analogue output signal for the converter circuit.

88.   A converter circuit according to claim 37 and any one of the claims 69-80, wherein the converter circuit has modules with combined logic operating CML circuits, and wherein for each module corresponding to bit k there is one corresponding combined logic operating circuit having a first current line, a second current line and a third current line, each said first current line being supplied from the same power supply via a first resistor network or via a first capacitor network having a first voltage output representing a first analogue output signal for the converter circuit, and each said third current line being supplied from said power supply via a second resistor network or via a second capacitor network having a

second voltage output representing a second analogue output signal for the converter circuit.

89.   A converter circuit according to claim 37 and any one of the claims 54-80,
wherein the converter circuit has modules with second logic operating CML circuits, and wherein for each module corresponding to bit m there is one corresponding CML circuit having a third current line and a fourth current line, each said third current line being supplied from the same power supply via a second resistor network or via a second capacitor network having a second voltage output representing a second analogue output signal for the converter circuit.

90.   A converter circuit according to any one of the claims 87-89, wherein the first resistor network is formed as a first R –2R network having the first voltage output.

91.   A converter circuit according to any of the claims 88-90, wherein the second resistor network is formed as a second R –2R network having the second voltage output.

92.   A converter circuit according to any one of the claims 79-91, wherein the second current lines of the CML circuits are powered by the positive terminal of the power supply or via a resistor connected to the positive terminal of the power supply.

93.   A converter circuit according to any one of the claims 79-92, wherein the converter circuit has second logic operating circuits, and wherein the fourth current lines of the second logic operating CML circuits are powered by the positive terminal of the power supply or via a resistor connected to the positive terminal of the power supply.

94.   A converter circuit according to claim 92 and 93, wherein the second current lines and the fourth current lines of the CML circuits are powered from the same supply line.

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95.   A converter circuit according to any one of the claims 79-94, wherein the constant current sources of the CML circuits are delivering current to the negative or ground terminal of the power supply.

5   96.   A converter according to any one of the claims 33-95, wherein the switching means of the CML circuits is made using N-MOS technology.

97.   A converter according to any one of the claims 33-91, wherein the switching means of the CML circuits is made using P-MOS technology.

10

98.   A phase-locked loop according to any one of the claims 6-9, wherein the converter circuit of the phase comparator comprises first AND operating circuits and second AND operating circuits for performing said first and second logic bit by bit operation, respectively, said first and second AND operating circuits being selected

15   from claims 48-51and claims 59-67 or selected from claims 48-51 and 59 and claims 79-82, 85-87, 89-97, and wherein the output of the first accumulator is the first digital signal, the inverted output of the second accumulator is the second digital signal, the inverted output of the first accumulator is the third digital signal, and the output of the second accumulator is the fourth digital signal.

20

99.   A phase-locked loop according to any one of the claims 6-9, wherein the converter circuit of the phase comparator comprises combined AND operating circuits for performing said first and second logic bit by bit operation, said combined AND operating circuits being selected from claims 73-78 or selected from claim 73

25   and claims 79-84, 88, 90-92, 95-97, and wherein the output of the first accumulator is the first digital signal, and the inverted output of the second accumulator is the second digital signal.

Fig. 1

Fig. 2

Fig. 3

Fig. 4

Fig. 5A


Fig. 5B

Fig. 6

Fig. 7

Fig. 8

925   926   916   915

Supply Voltage

$I_{Down}{}^k$ $I_{Up}{}^k$

931   Vbias   930   Vbias

$\overline{N_{V_k}}$ N_{V_k}

N_{V_k} $\overline{N_{V_k}}$

921   911

$\overline{N_{R_k}}$ N_{R_k}

923   922   912   913

917   910
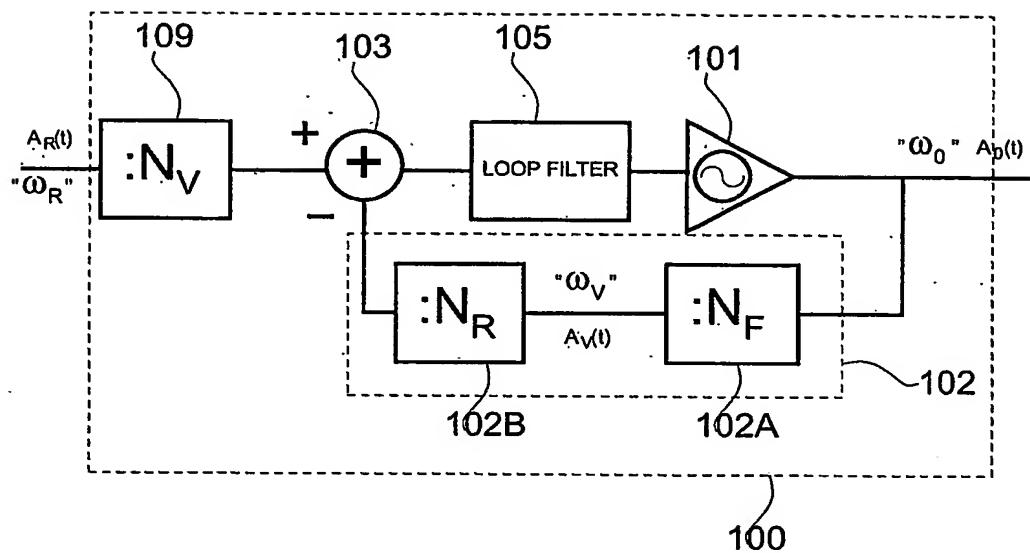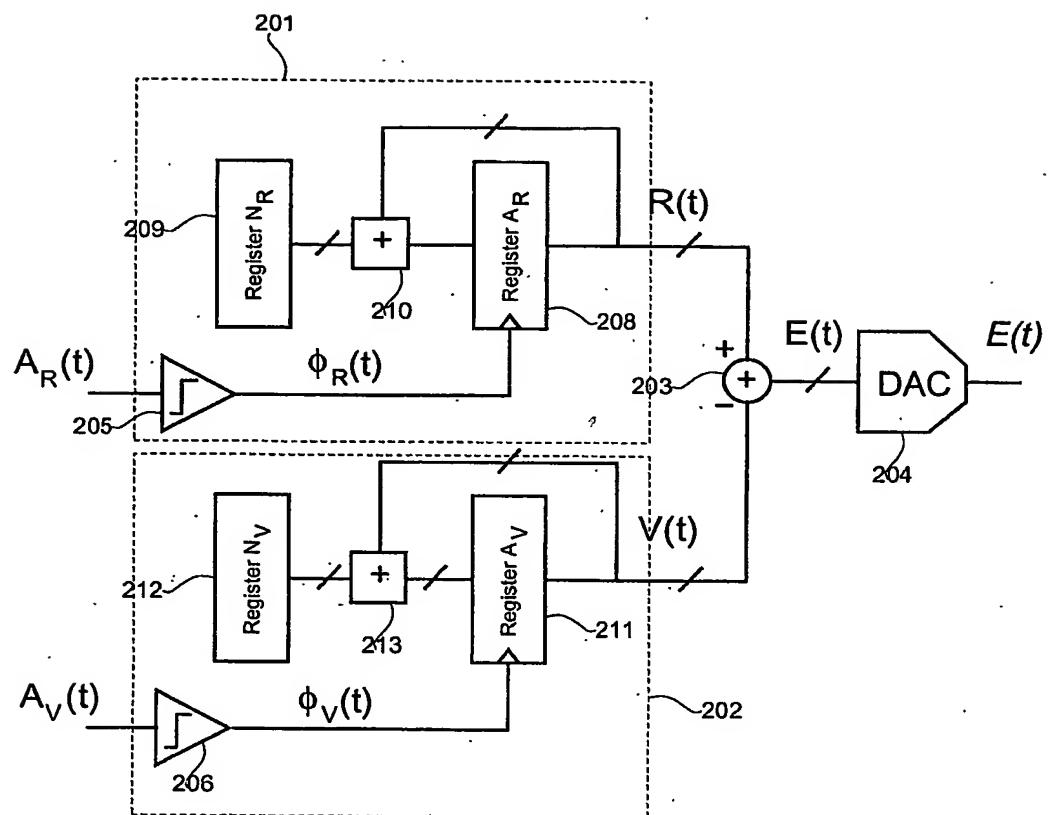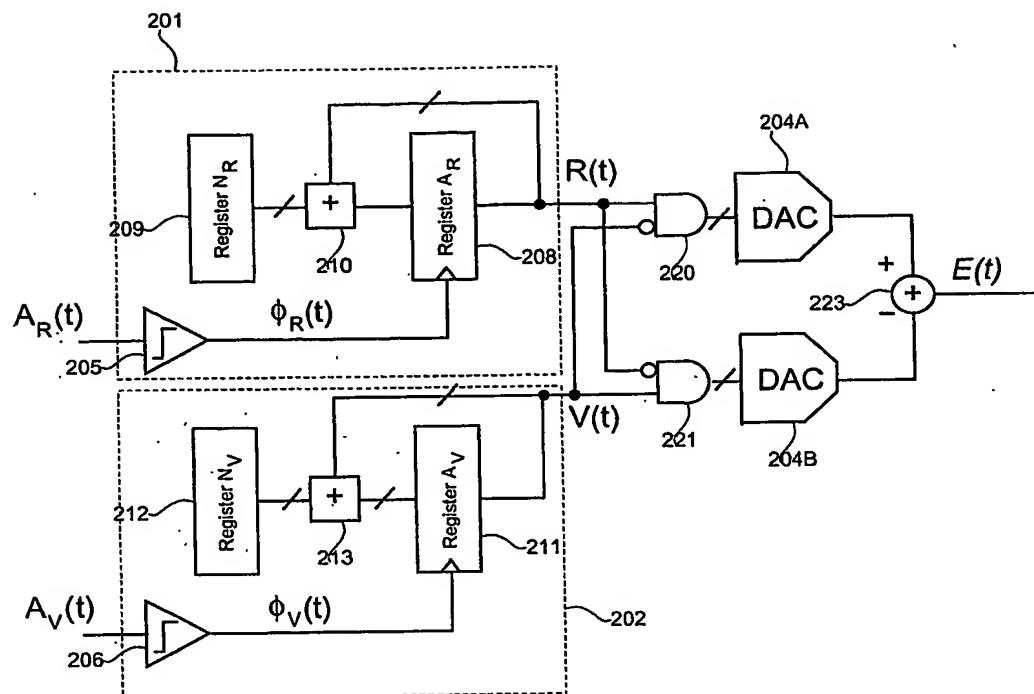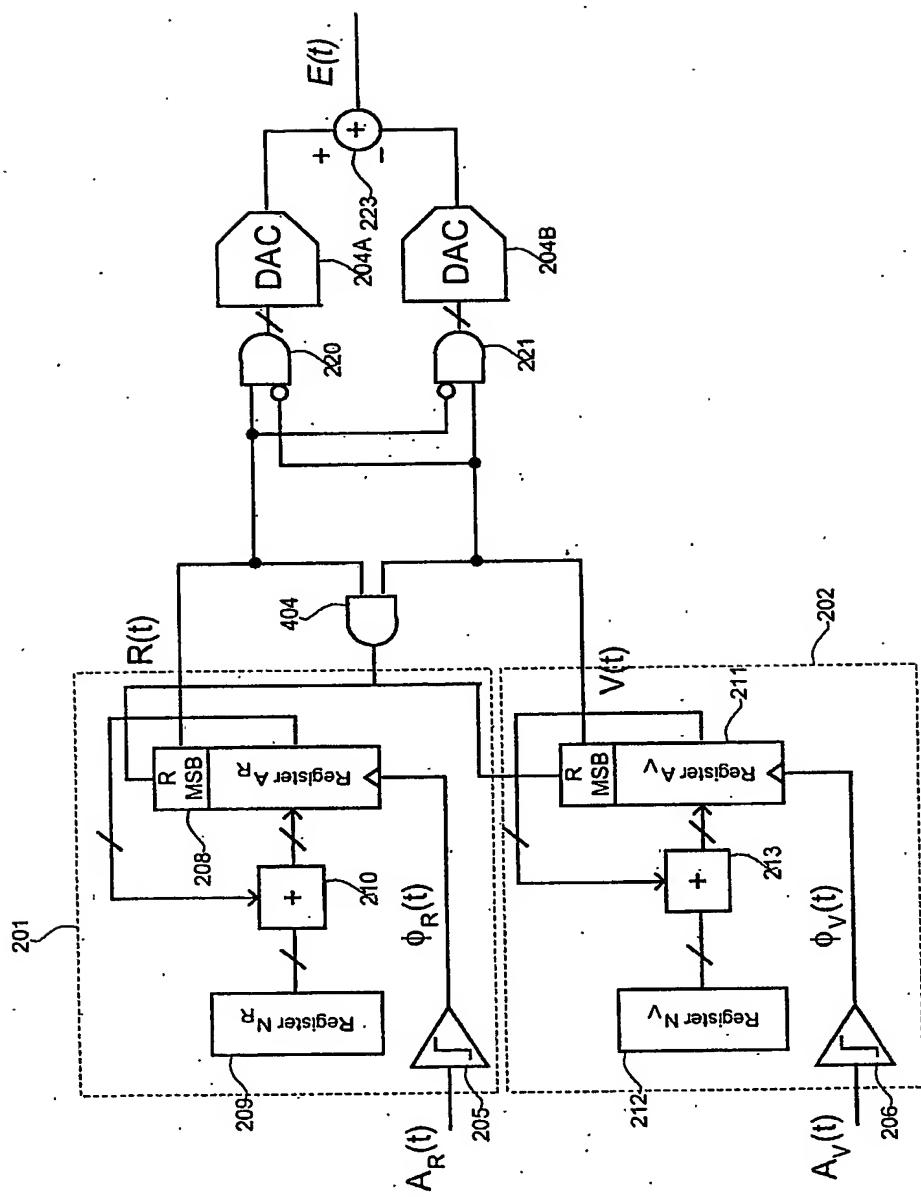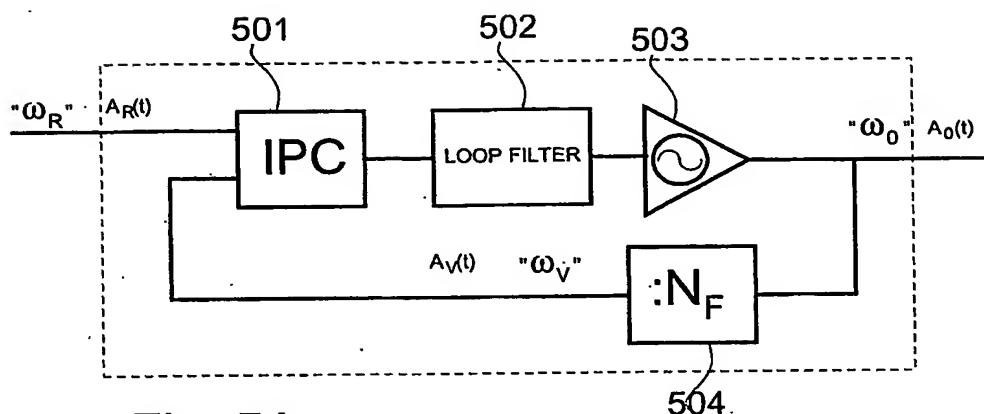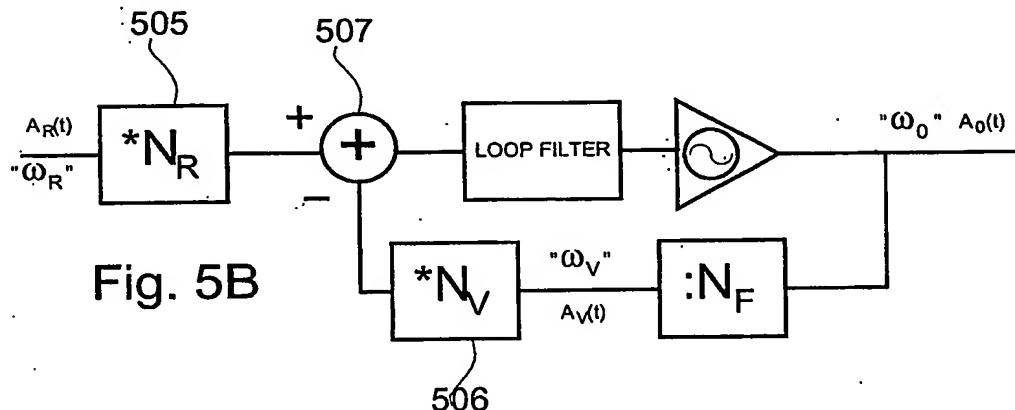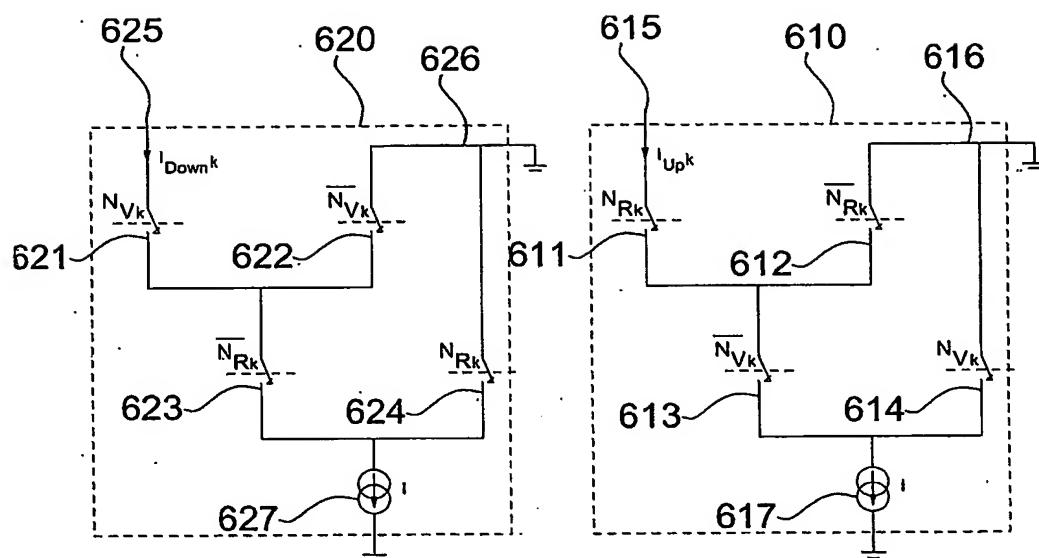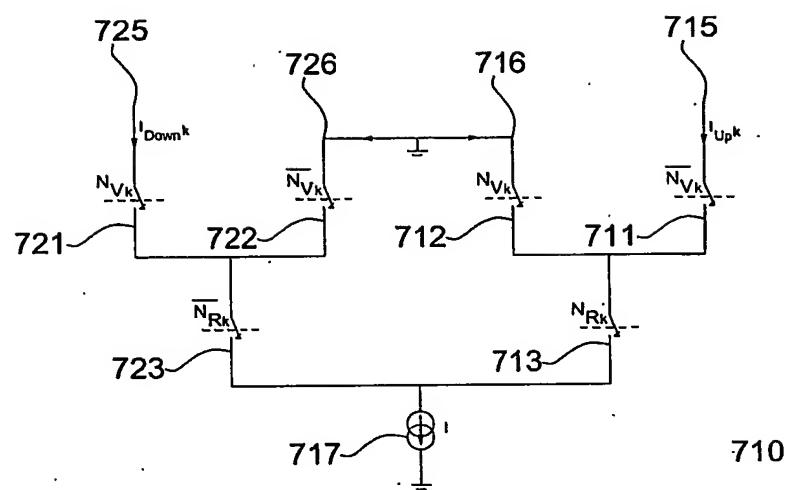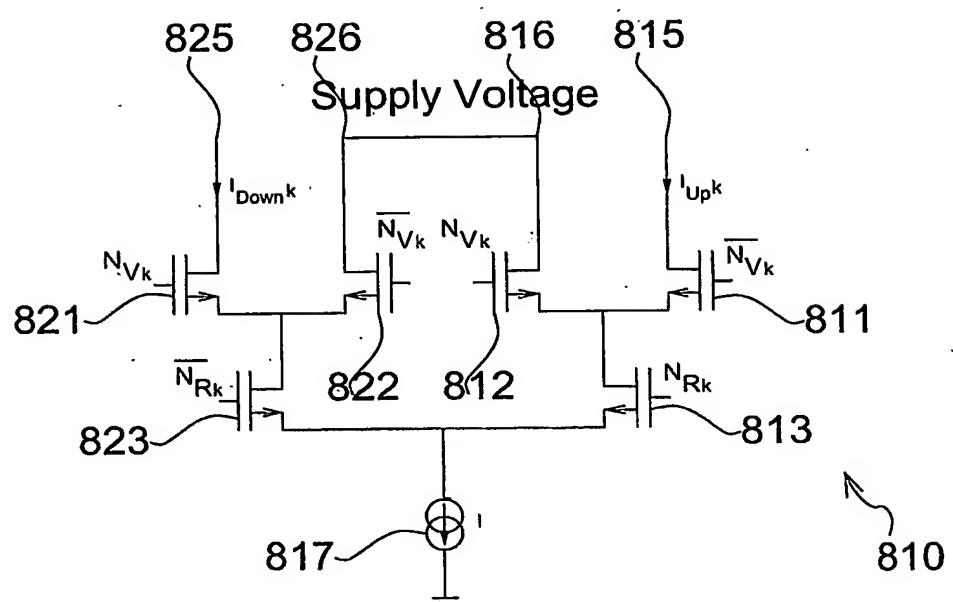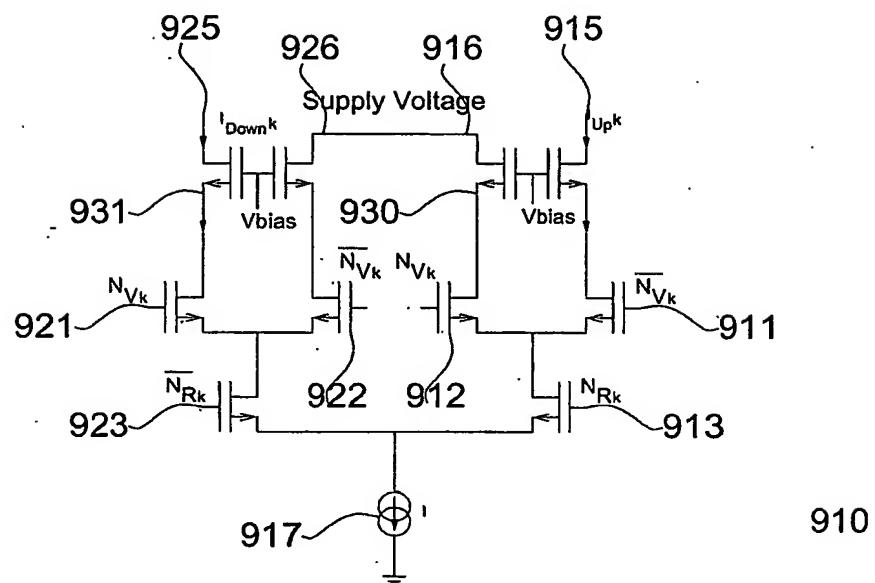
Fig. 9
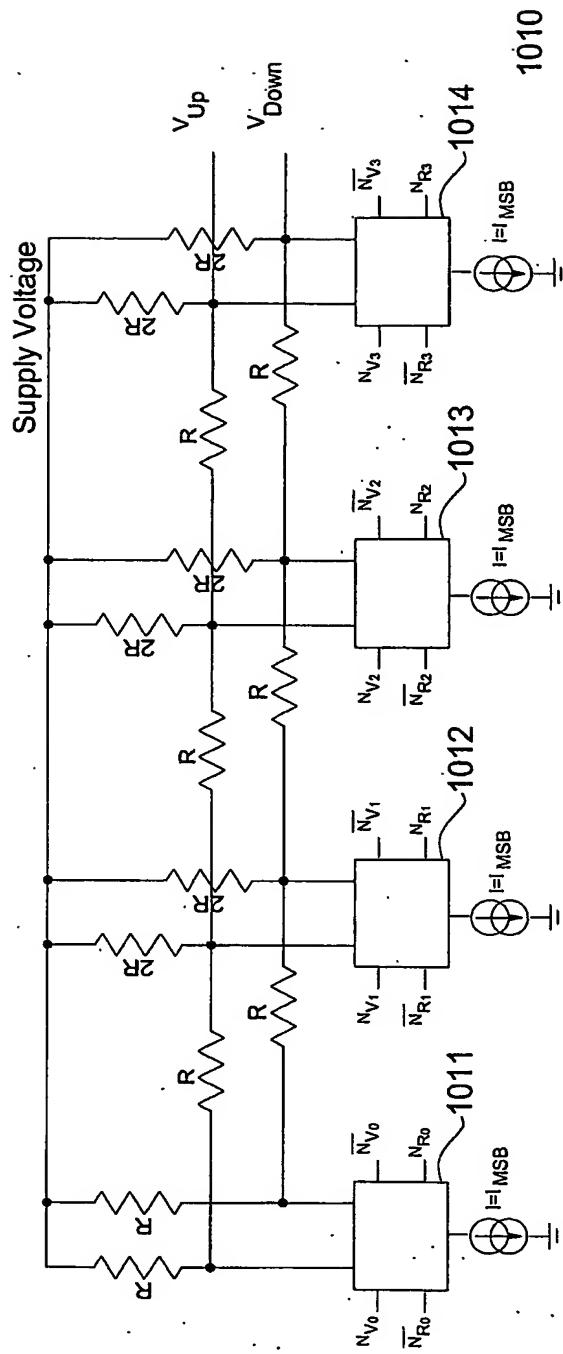
Fig. 10
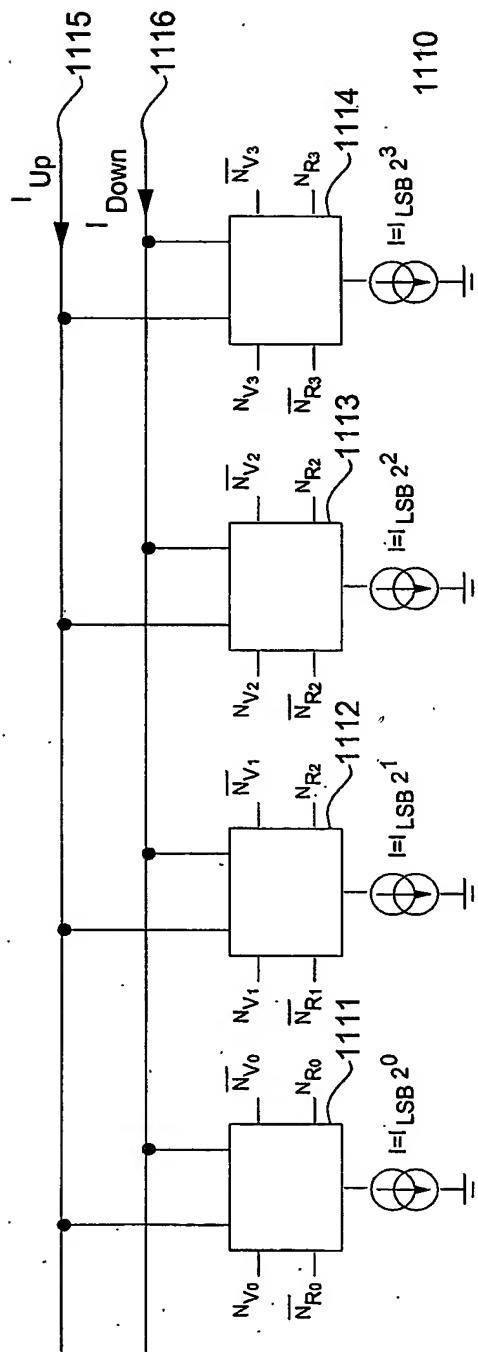
Fig. 11
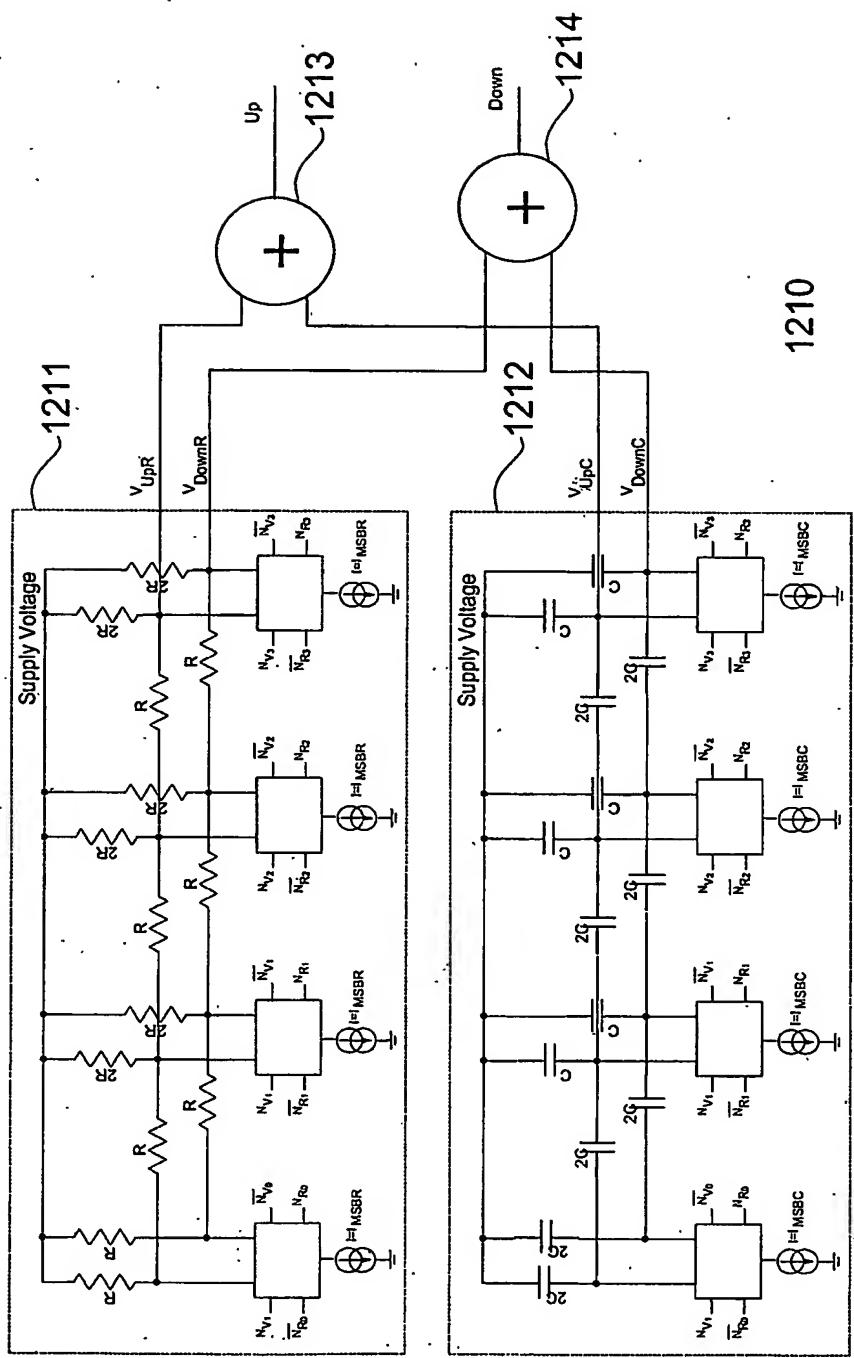
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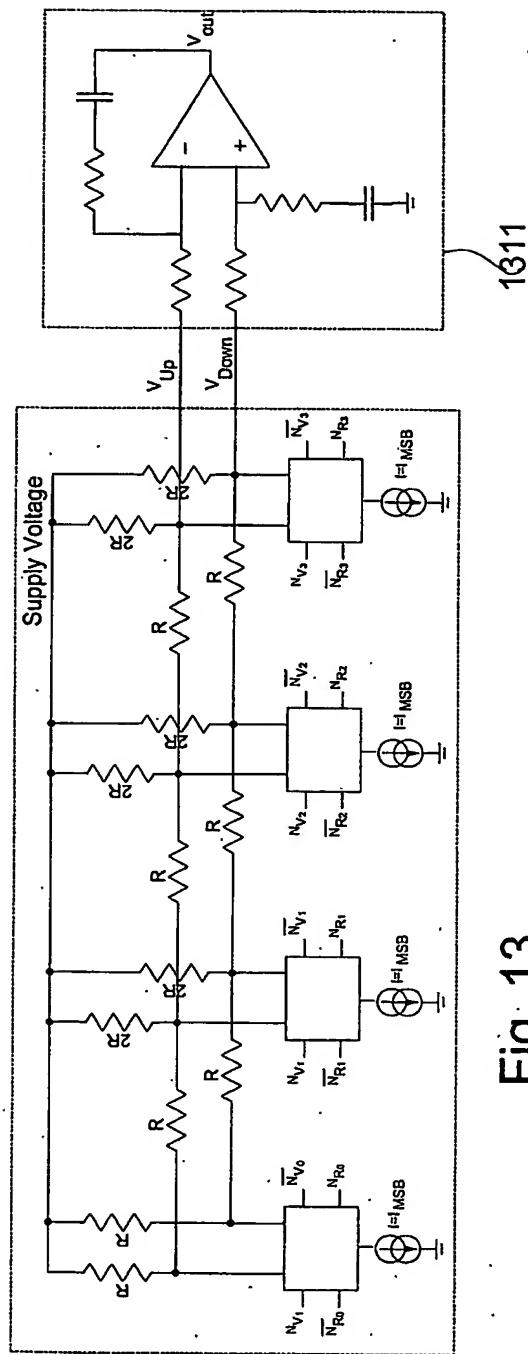
Fig. 13
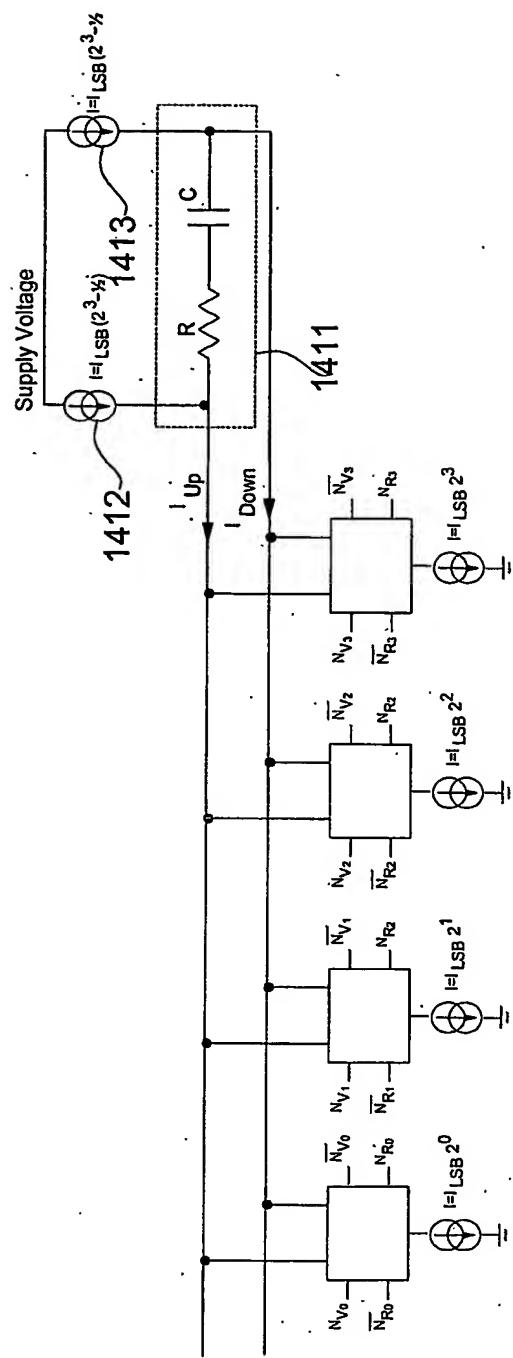
Fig. 14

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03L7/085

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 317 283 A (KORHONEN VEIJO S) 31 May 1994 (1994-05-31) the whole document ---	1-99
A	US 5 373 255 A (BRAY JEFFREY P ET AL) 13 December 1994 (1994-12-13) the whole document ---	1-99
A	US 5 909 130 A (MARTIN DAVID G ET AL) 1 June 1999 (1999-06-01) the whole document ---	1-99
A	US 5 656 976 A (JUNG YOUNG-JU ET AL) 12 August 1997 (1997-08-12) the whole document -----	1-99

| | Further documents are listed in the continuation of box C. | | [X] | Patent family members are listed in annex. |

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 October 2003	11. 11. 2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Stefan Hultquist

Form PCT/ISA/210 (second sheet) (July 1992)

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5317283	A	31-05-1994	GB	2278969 A ,B	14-12-1994
			JP	7030417 A	31-01-1995
US 5373255	A	13-12-1994	EP	0637137 A2	01-02-1995
			JP	3299636 B2	08-07-2002
			JP	7095060 A	07-04-1995
US 5909130	A	01-06-1999	NONE		
US 5656976	A	12-08-1997	KR	9616812 B1	21-12-1996

PATENT COOPERATION TREATY

RECD **15 DEC 2004**

WIPO   PCT

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference P775PC00	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)

International application No. PCT/DK 03/00404	International filing date *(day/month/year)* 18.06.2003	Priority date *(day/month/year)* 19.06.2002

International Patent Classification (IPC) or both national classification and IPC H03L7/085

Applicant R & C Holding ApS et al.

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

    ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

    These annexes consist of a total of 5 sheets.

3. This report contains indications relating to the following items:

    I   ☒ Basis of the opinion

    II ☐ Priority

    III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

    IV ☐ Lack of unity of invention

    V   ☒ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

    VI ☐ Certain documents cited

    VII ☐ Certain defects in the international application

    VIII ☐ Certain observations on the international application

Date of submission of the demand 16.01.2004	Date of completion of this report 13.12.2004

Name and mailing address of the International preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Nicolaucig, A Telephone No. +49 89 2399-7670

INTERNATIONAL PRELIMINARY
EXAMINATION REPORT

International application No.   PCT/DK 03/00404

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17)):*

Description, Pages

1-49   as published

Claims, Numbers

1-18   received on 28.10.2004 with letter of 25.10.2004

Drawings, Sheets

1/14-14/14   as published

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: . , which is:

   ☐   the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).

   ☐   the language of publication of the international application (under Rule 48.3(b)).

   ☐   the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   ☐   contained in the international application in written form.

   ☐   filed together with the international application in computer readable form.

   ☐   furnished subsequently to this Authority in written form.

   ☐   furnished subsequently to this Authority in computer readable form.

   ☐   The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   ☐   The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   ☐   the description,   pages:

   ☐   the claims,   Nos.:

   ☐   the drawings,   sheets:

5. ☐   This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-18
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-18
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-18
	No:	Claims	

2. Citations and explanations

   see separate sheet

<u>**Re Item V**</u>
Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1   Reference is made to the following documents:

D1:   US-A-6046643
D2:   US-A-6075387

2   The document D1 is regarded as being the closest prior art to the subject-matter of claim 1, and shows (the references in parentheses applying to this document):

a method (see figure) for determining a phase error (output of D/A) in response to a first signal (fref, clock input of ACCU2) and a second signal (clock input of ACCU1), said method comprising the steps of:

generating a first reoccurring trigger event (rising/falling edge on clock input of ACCU2) in response to the first signal;

generating a second reoccurring trigger event (rising/falling edge on clock input of ACCU1) in response to the second signal,

incrementing (col. 3, l. 18-20) a first phase value by a first predetermined increment value (aref) when the first trigger event occurs to obtain a first accumulated phase value (output of ACCU2) represented by a binary number,

incrementing a second phase value (col. 3, l. 17-18) by a second predetermined increment value when the second trigger event occurs to obtain a second accumulated phase value (output of ACCU1) represented by a binary number, and

calculating or determining (through H1, H3 and D/A) said phase error based on obtained first and second accumulated phase values, said phase error being represented by a binary number (output of D/A) or one or more analogue signals (input of D/A).

2.1   The subject-matter of claim 1 differs from this known method for determining a phase

error in that

said method further comprises the steps of
resetting the most significant bit of the first accumulated phase value and the most significant bit of the second accumulated phase value when the most significant bit of both said first accumulated phase value and said second accumulated phase value are simultaneously 1.

2.2 The subject-matter of claim 1 is therefore novel (Article 33(2) PCT).

2.3 The problem to be solved by the present invention may be regarded as avoiding an overflow of the accumulated phase and making it easier to obtain a difference between the two accumulated phase values.

2.4 The solution to this problem proposed in claim 1 of the present application is considered as involving an inventive step (Article 33(3) PCT) for the following reasons:

there is no hint in D1 or D2 to the problem of overflowing of the accumulated phase value nor to the proposed solution. The person skilled in the art would not arrive to such a solution without exercising an inventive step.

2.5 The same arguments apply mutatis mutandis to independent claim 8, defining corresponding phase-locked loop, and independent claim 14, defining corresponding phase comparator, so that they also meet the requirements of the PCT with respect to novelty and inventive step.

2.6 Claims 2-7, 9-13, 15-18 are dependent on claims 1, 8 or 14, and as such also meet the requirements of the PCT with respect to novelty and inventive step.

3 The subject-matter of claims 1-18 is industrially applicable.

CLAIMS filed in response to the first written opinion

1.   A method for determining a phase error in response to a first signal and a second signal, said method comprising the steps of:

5   generating a first reoccurring trigger event in response to the first signal,

generating a second reoccurring trigger event in response to the second signal,

incrementing a first phase value by a first predetermined increment value when the first trigger event occurs to obtain a first accumulated phase value represented by a binary number,

10   sented by a binary number,

incrementing a second phase value by a second predetermined increment value when the second trigger event occurs to obtain a second accumulated phase value represented by a binary number, and

calculating or determining said phase error based on obtained first and second accumulated phase values, said phase error being represented by a binary number or one or more analogue signals,

15   accumulated phase values, said phase error being represented by a binary number or one or more analogue signals,

said method further comprising the steps of

resetting the most significant bit of the first accumulated phase value and the most significant bit of the second accumulated phase value when the most significant bit of both said first accumulated phase value and said second accumulated phase value are simultaneously 1.

20   cant bit of both said first accumulated phase value and said second accumulated phase value are simultaneously 1.

2.   A method according to claim 1, wherein the phase error is represented by one or more an analogue signals.

25

3.   A method according to claim 2, said method further comprising the steps of:

performing a first logic bit by bit AND operation of the first accumulated phase value and the inverted second accumulated phase value, and generating a first analogue representation of said first logic bit by bit AND operation, and

30   performing a second logic bit by bit AND operation of the second accumulated phase value and the inverted first accumulated phase value, and generating a second analogue representation of said second logic bit by bit AND operation.

4.   A method according to claim 3, wherein the calculation of the phase error

35   comprises generating one or more analogue phase error signal based on the sec-

ond analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

5. A method according to claim 4, wherein the calculation of the phase error comprises performing an analogue subtraction of the second analogue representation from the first analogue representation.

6. A method according to any one of the claims 1-5, wherein two equal bits are reset whenever these bits are 1 at the same time.

7. A method according to any one of the claims 1-6, said method comprising the step of frequency dividing the first signal and/or the second signal, whereby the generation of the first and/or second reoccurring trigger event is performed in response to the frequency divided first and/or second signal, respectively.

8. A phase-locked loop comprising:
a voltage controlled oscillator for generating an output signal and having a frequency control input for controlling the frequency of the output signal, and
a phase comparator for deriving a control signal from a phase error detected in response to the received output signal and a reference signal, said control signal being coupled to the frequency control input of said voltage controlled oscillator, wherein the phase comparator includes:
a first accumulator adapted to add a first predefined phase step value to a first accumulated phase value in response to a reoccurring event in the reference signal,
a second accumulator adapted to add a second predefined phase step value to a second accumulated phase value in response to a reoccurring event in the received output signal, and
means or arithmetic means for determining the phase error from the obtained first and second accumulated phase values,
said phase comparator further including a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator, and a third AND-means, where the output of said third AND-means is connected to said first and said second reset means of said first and said second accumulator, where the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the

most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means.

9.   A phase-locked loop according to claim 8, wherein the phase comparator includes a converter circuit having:

means for performing a first logic bit by bit AND operation of the output of the first accumulator and the inverted output of the second accumulator, and for generating a first analogue representation of said first logic bit by bit AND operation, and

means for performing a second logic bit by bit AND operation of the output of the second accumulator and the inverted output of the first accumulator, and for generating a second analogue representation of said second logic bit by bit AND operation.

10.   A phase-locked loop according to claim 9, wherein the converter circuit comprises current mode logic circuits giving a current output for a two input AND operation, said current output being used for generating an analogue representation for a bit by bit AND operation.

11.   A phase-locked loop according to claim 9 or 10, wherein the arithmetic means are adapted to obtain one or more analogue phase error signals based on the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

12.   A phase-locked loop according to claim 11, wherein the arithmetic means comprises subtraction means being adapted for performing an analogue subtraction of the second analogue representation from the first analogue representation.

13.   A phase-locked loop according to any one of the claims 8-12, further comprising a divider for dividing the frequency of the output signal, whereby the received output signal received by the phase comparator is a frequency-divided output signal.

14.   A phase comparator for carrying out the method in accordance to claim 1-7, wherein the first signal is a reference signal and the second signal is an input signal, said phase comparator including:

a first accumulator adapted to add a first predefined phase step value to a first accumulated phase value in response to a reoccurring event in said reference signal,

a second accumulator adapted to add a second predefined phase step value to a second accumulated phase value in response to a reoccurring event in said input signal, and

means or arithmetic means for determining the phase error based on the second accumulated phase value and the first accumulated phase value,

said phase comparator further including a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator and a third AND-means, where the output of said third AND-means is connected to said first and said second reset means of said first and said second accumulator, where the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means.

15.   A phase comparator according to claim 14, wherein the phase comparator includes a converter circuit having:

means for performing a first logic bit by bit AND operation of the output of the first accumulator and the inverted output of the second accumulator, and for generating a first analogue representation of said first logic bit by bit AND operation, and

means for performing a second logic bit by bit AND operation of the output of the second accumulator and the inverted output of the first accumulator, and for generating a second analogue representation of said second logic bit by bit AND operation.

16.   A phase comparator according to claim 15, wherein the converter circuit comprises current mode logic circuits giving a current output for a two bit AND operation, said current output being used for generating an analogue representation for a bit by bit AND operation.

17.   A phase comparator according to claim 15 or 16, wherein the arithmetic means are adapted to obtain one or more analogue phase error signals based on

the second analogue representation of the second logic bit by bit AND operation and the first analogue representation of the first logic bit by bit AND operation.

18. A phase comparator according to claim 17, wherein the arithmetic means comprises subtraction means being adapted for performing an analogue subtraction of the second analogue representation from the first analogue representation.

Box No. VIII (iv)   DECLARATION: INVENTORSHIP (only for the purposes of the designation of the United States of America)

The declaration must conform to the following standardized wording provided for in Section 214; see Notes to Boxes Nos. VIII, VIII (i) to (v) (in general) and the specific Notes to Box No. VIII (iv). If this Box is not used, this sheet should not be included in the request.

Declaration of inventorship (Rules 4.17(iv) and 51bis.1(a)(iv))
for the purposes of the designation of the United States of America:

I hereby declare that I believe I am the original, first and sole (if only one inventor is listed below) or joint (if more than one inventor is listed below) inventor of the subject matter which is claimed and for which a patent is sought.

This declaration is directed to the international application of which it forms a part (if filing declaration with application).

This declaration is directed to international application No. PCT/ DK03/00404 .... (if furnishing declaration pursuant to Rule 26ter).

I hereby declare that my residence, mailing address, and citizenship are as stated next to my name.

I hereby state that I have reviewed and understand the contents of the above-identified international application, including the claims of said application. I have identified in the request of said application, in compliance with PCT Rule 4.10, any claim to foreign priority, and I have identified below, under the heading "Prior Applications," by application number, country or Member of the World Trade Organization, day, month and year of filing, any application for a patent or inventor's certificate filed in a country other than the United States of America, including any PCT international application designating at least one country other than the United States of America, having a filing date before that of the application on which foreign priority is claimed.

Prior Applications: Danish patent application No. PA 2002 00933 filed 19 June 2002 ....

I hereby acknowledge the duty to disclose information that is known by me to be material to patentability as defined by 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the PCT international filing date of the continuation-in-part application.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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(if not contained in the request, or if declaration is corrected or added under Rule 26ter after the filing of the international application. The signature must be that of the inventor, not that of the agent)   (of signature which is not contained in the request, or of the declaration that is corrected or added under Rule 26ter after the filing of the international application)

Name: ....

Residence: ....
(city and either US state, if applicable, or country)

Mailing Address: ....

Citizenship: ....

Inventor's Signature: ....   Date: ....
(if not contained in the request, or if declaration is corrected or added under Rule 26ter after the filing of the international application. The signature must be that of the inventor, not that of the agent)   (of signature which is not contained in the request, or of the declaration that is corrected or added under Rule 26ter after the filing of the international application)

☐ This declaration is continued on the following sheet, "Continuation of Box No. VIII (iv)".

Form PCT/RO/101 (declaration sheet (iv)) (March 2001; reprint January 2002)   *See Notes to the request form*